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(54) Semiconductor integrated circuits/systems

(57) Configurable semiconductor integrated circuits as-made each have a plurality of logic circuits formed at discrete sites (10S). For each logic circuit, direct selectably conducting/non-conducting connection paths (14A,B,C,F) extend from its output to input of a first set of other logic circuits and to its inputs from outputs of a second set of other logic circuits. All of the sets for all of the logic circuits are each different. Other direct connection paths (50R,50C) are selectably connectable to inputs (14D,E) and outputs (52G,H) of the logic circuits. Selection can be irreversible (Fig. 8) or reversible (Figs. 9, 10, 11, 18) and involves coincident signal addressing (22R,C) of the sites (10S) and coded configuring of the paths at that site. Reversible selection can be via field effect transistors or bipolar transistors and can be at or near normal logic signal levels and speeds (Figs. 11 and 18). Versatile configurable input/output arrangements are described (Figs. 13–16), also reconfigurable data processing systems using the reversible transistor provisions (Figs.
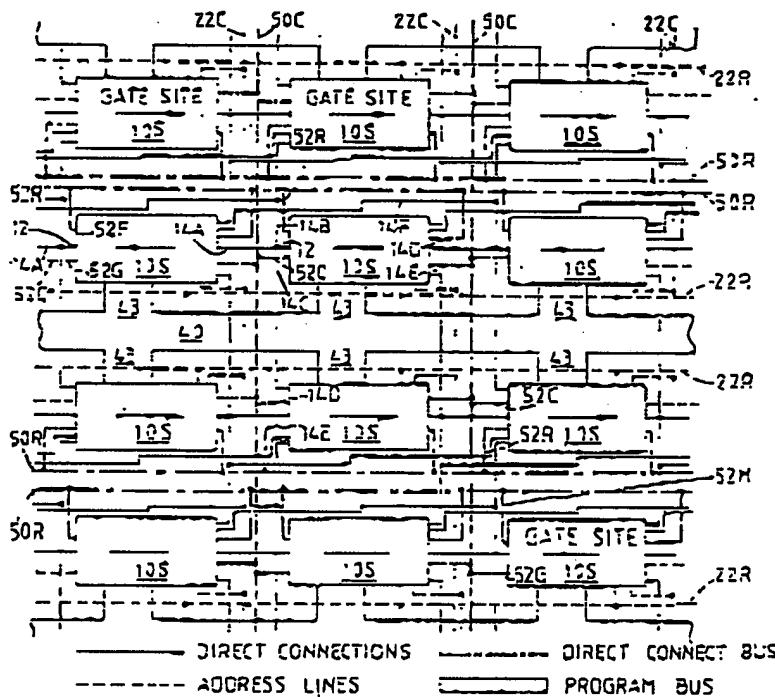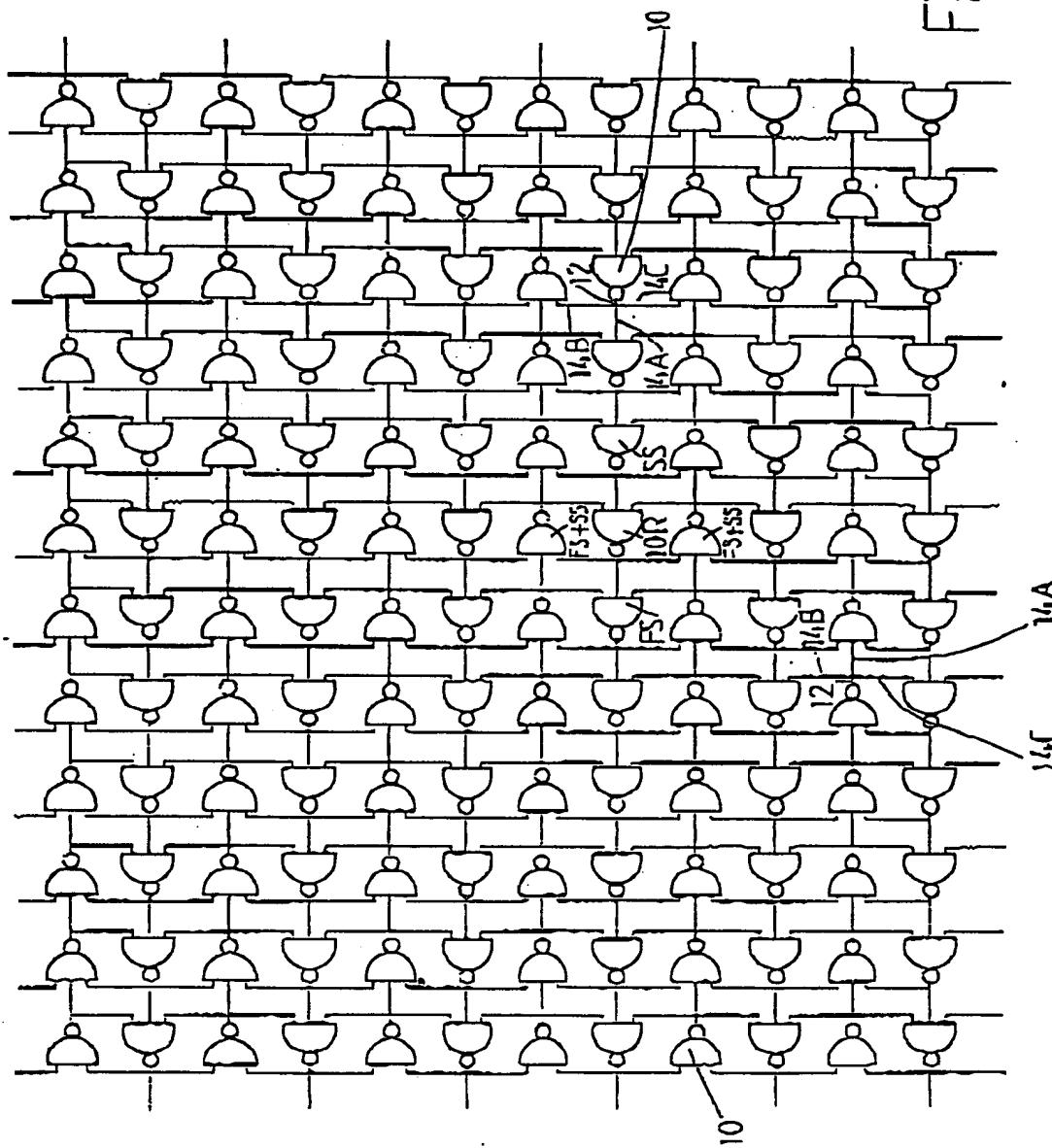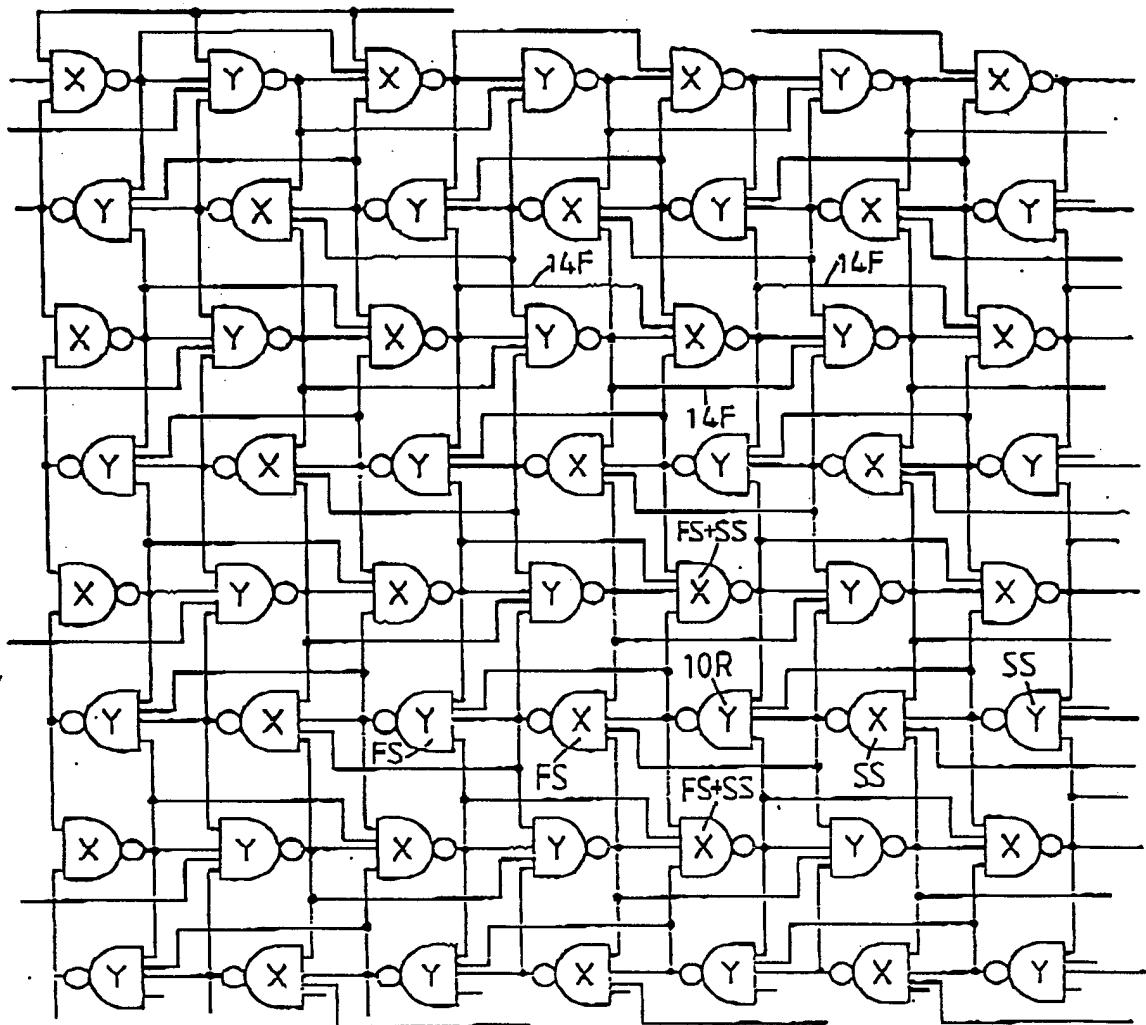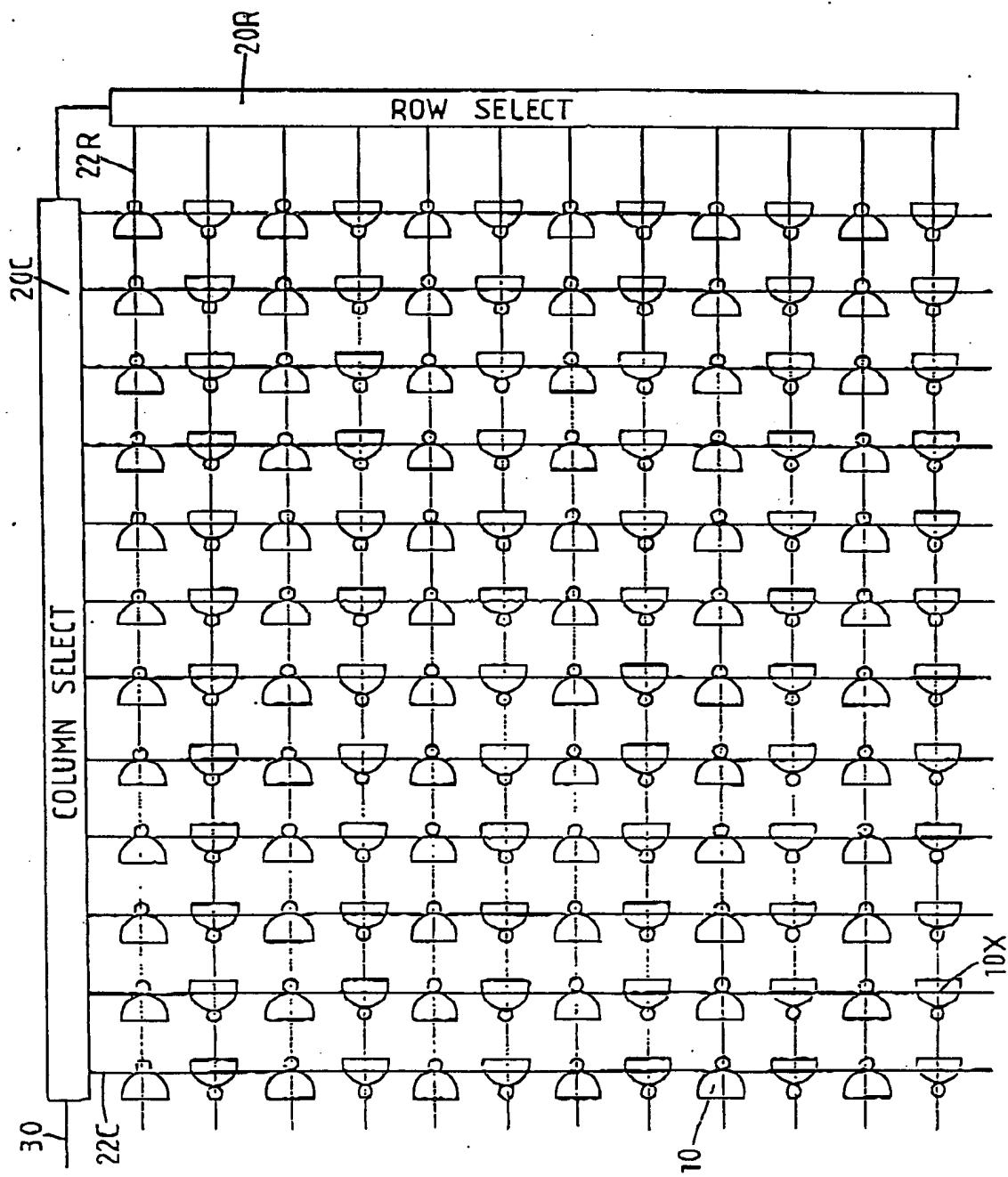
DIRECT CONNECTIONS ——— DIRECT CONNECT BUS
ADDRESS LINES ———— PROGRAM BUS

FIG.7

FIG.1.

FIG.2.

FIG.3

FIG.4.

FIG.5.

FIG.6.

53A

10A	10A	10A	10A	10A
10Z	10Z	10Z	10Z	10Z
10B	10B	10B	10B	10B

53B

FIG.6A.

22C 50C 22C 50C 22C

22R

GATE SITE 10S

GATE SITE 52R 10S

10S

50R

50R

52R

12 52F 14A 14B 14F

14A 52G 10S 12 14D

52C 10S 52C 10S 14E

22R

14C

52C 43 14C 43 43

40

43 43 43

22R

14D 52C

10S 14E 10S 52R 10S

50R

52H

50R 10S 10S GATE SITE 52G 10S

22R

——————— DIRECT CONNECTIONS ——·——·—— DIRECT CONNECT BUS

— — — — ADDRESS LINES [▭] PROGRAM BUS

FIG.7.

FIG.8.

FIG.9.

FIG.10.

FIG.11.

FIG.12.

FIG.13.

FIG.14.

PERIPHERAL CELL

PERIPHERAL CELL

PERIPHERAL CELL

PERIPHERAL CELL

LOGIC ARRAY MATRIX

300

320B
326C
320C
310B
310C
310D
326B
326D
310A
320A
326A
320D

VDD.1 C5 R0 R3 R4

DA1 ─
QA1 ─   ─ PA1

DA20 ─
QA20 ─   ─ PA20

VSS VDD2   DB0-DB7

310

FIG.15

330   332   336

DA1 ─▷○ PCELL   ─ PA1

            VDD2

QA1 ─○▷ PCELL
      334

X20   338

R4 C5 DB0

FIG.16.

FIG.17A.

FIG.17B.

FIG.18

FIG.19.

FIG.20.

622 604 ADDRESS 604A 610

I/O MEANS 620

LOGIC 600

RAM 602

610B

SYSTEMS 608

610A

606 606A

DATA

FIG.21.

612 616

MUX

ADDRESS

604

644 642

622

LOGIC 600

RAM 602

648

640

I/O

630

646

680

606 MUX 618 DATA

614

FIG.22.

830

800   800   800

805   805   805

805   805

820   800   800   800   910

825   815

805   805   805

805   805

800   800   800
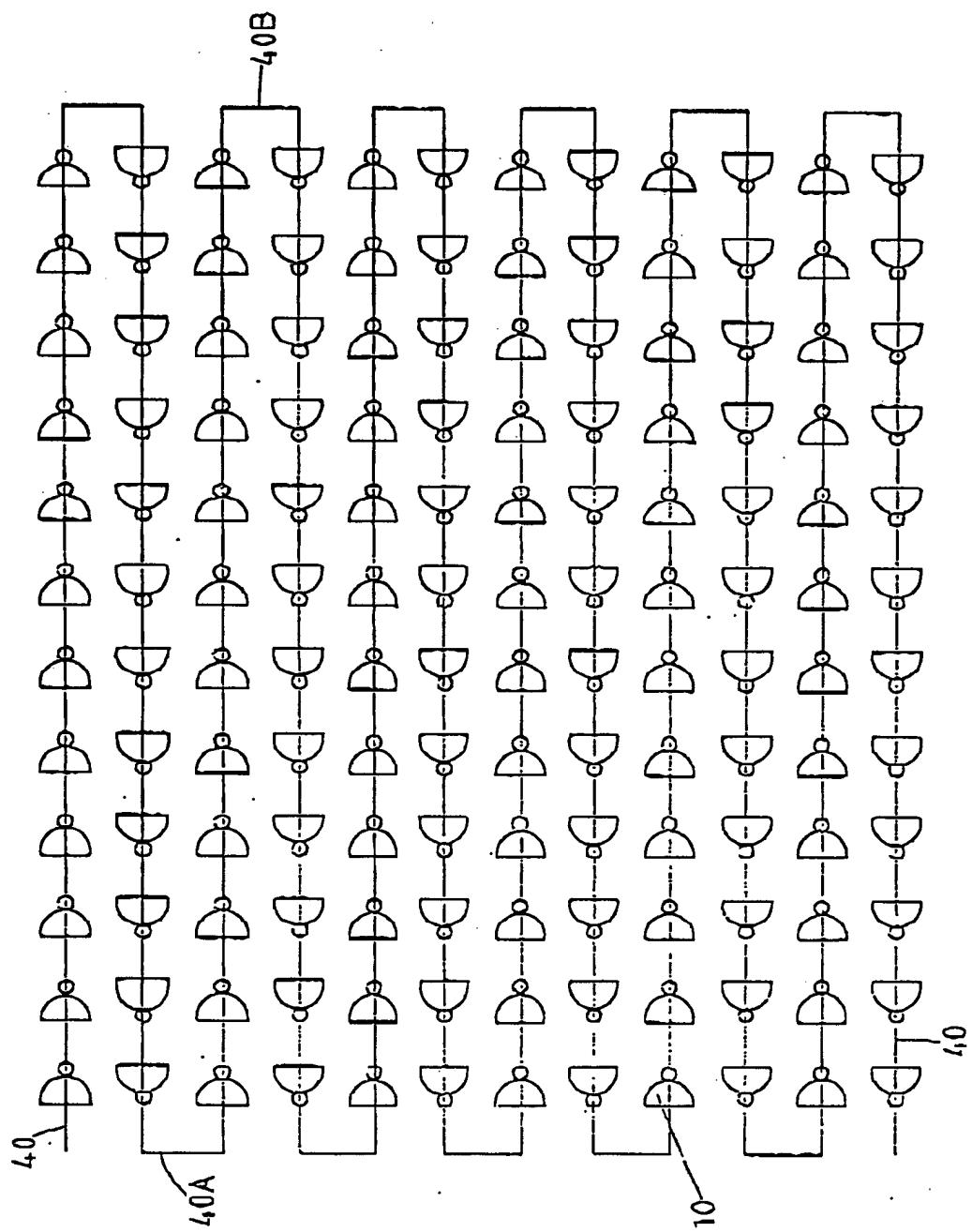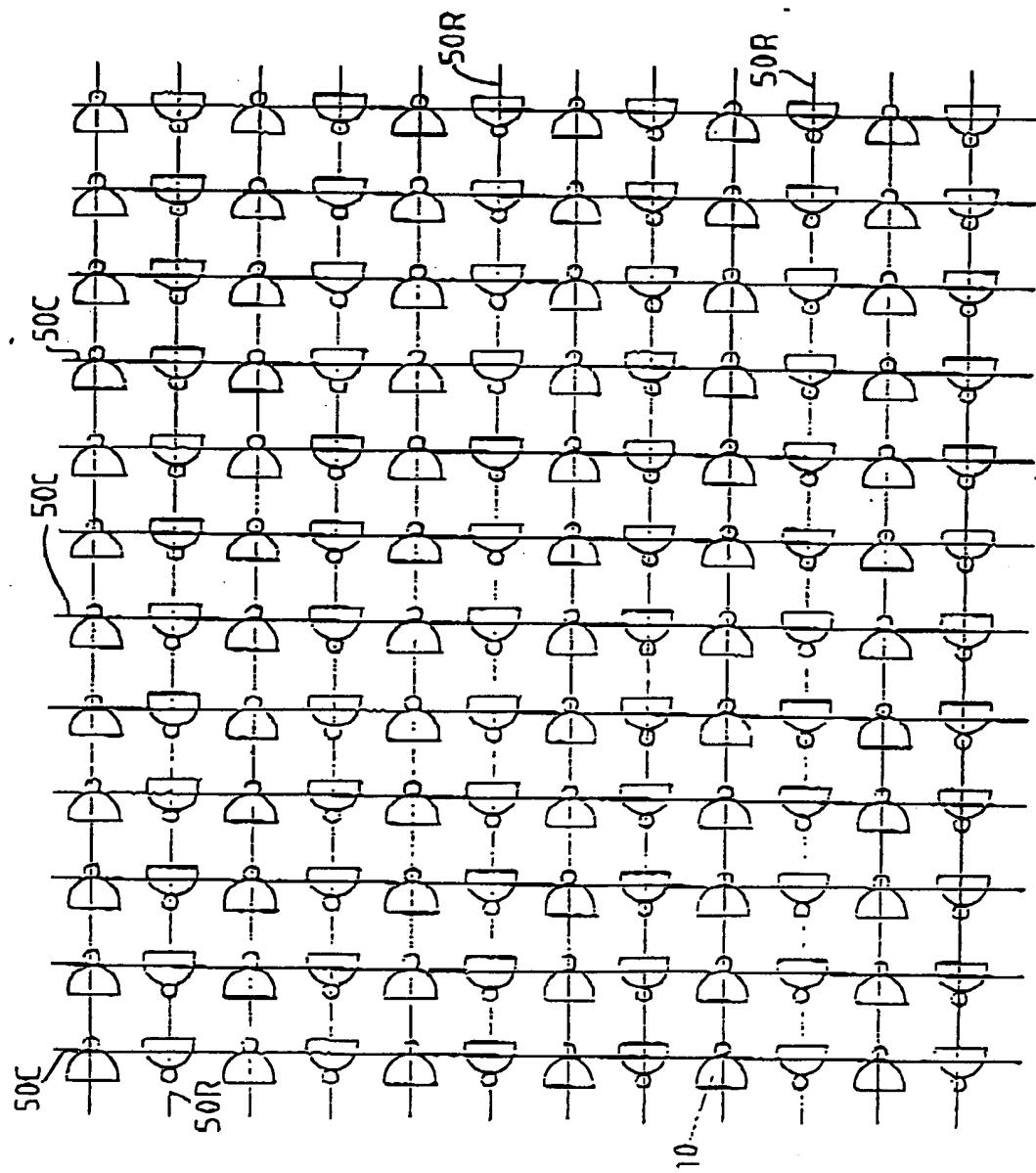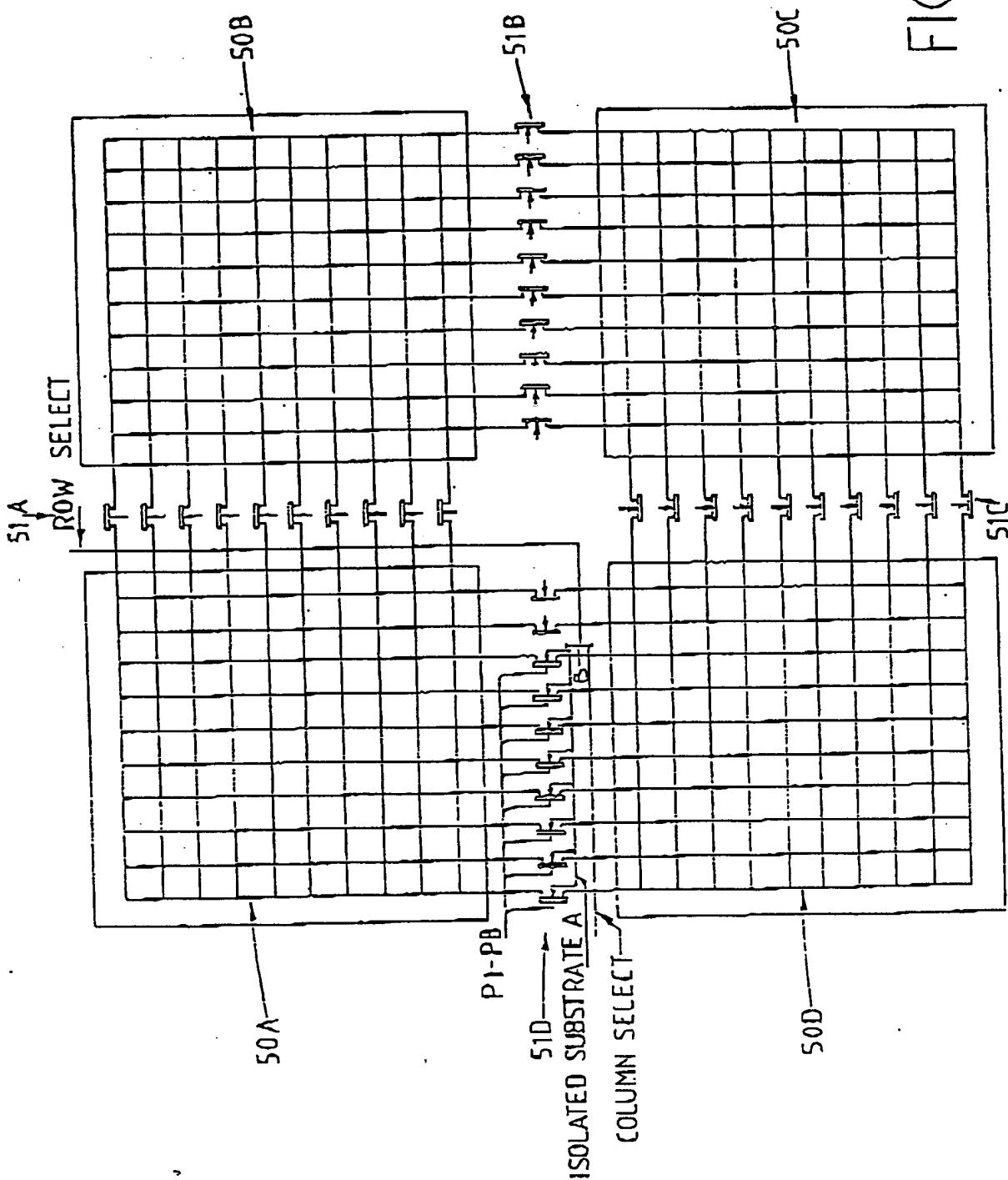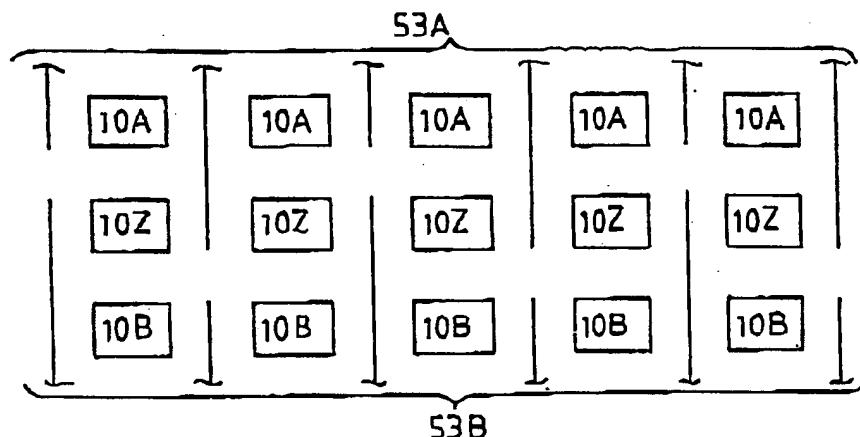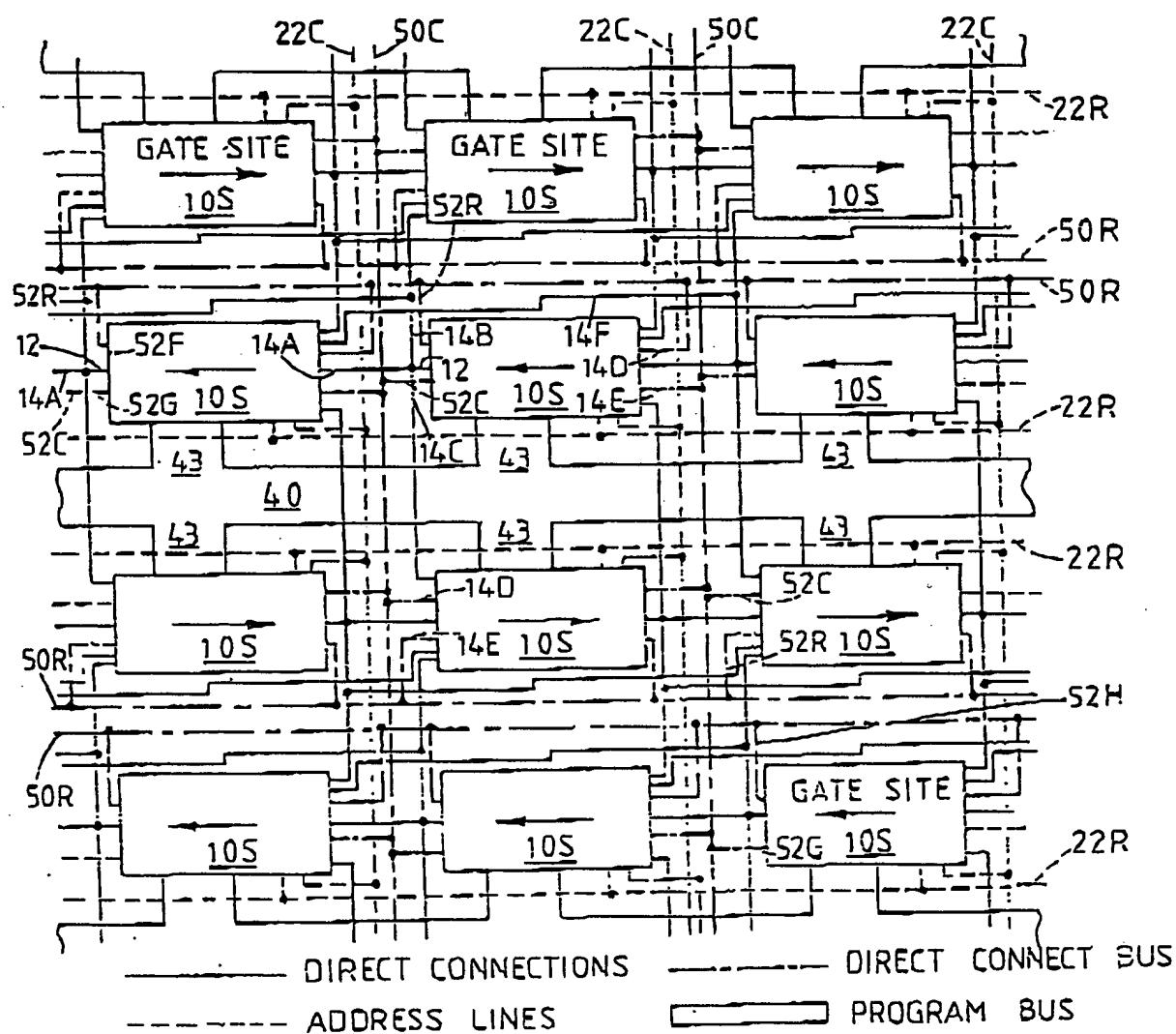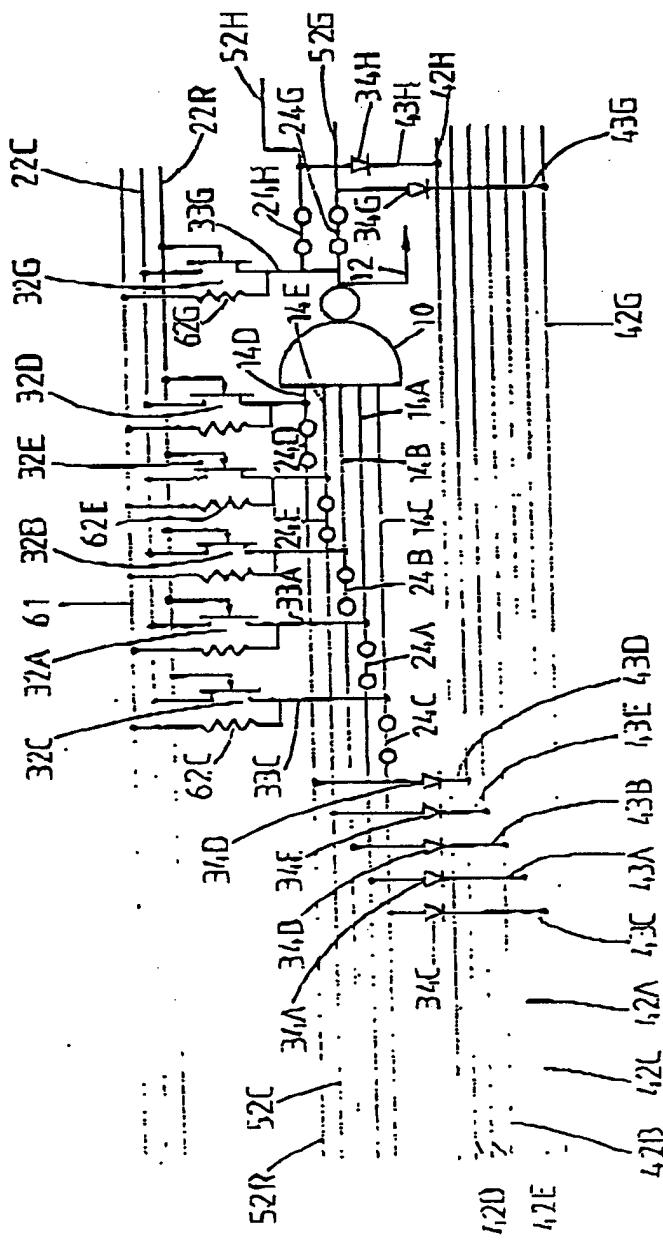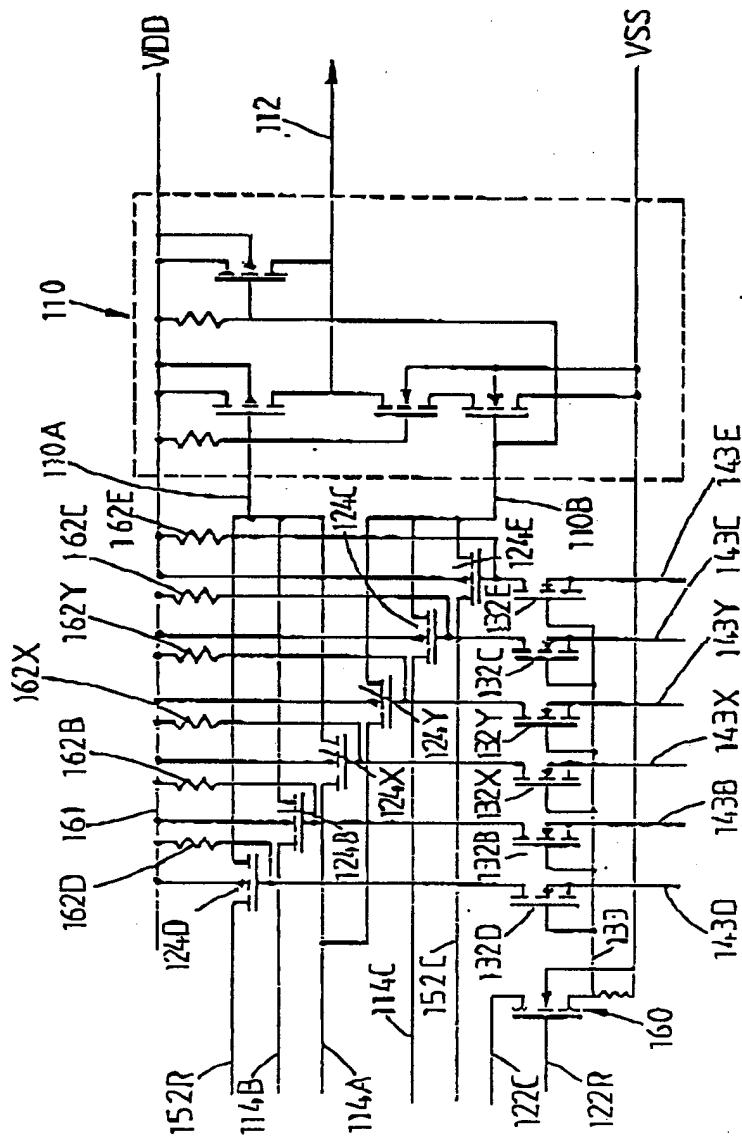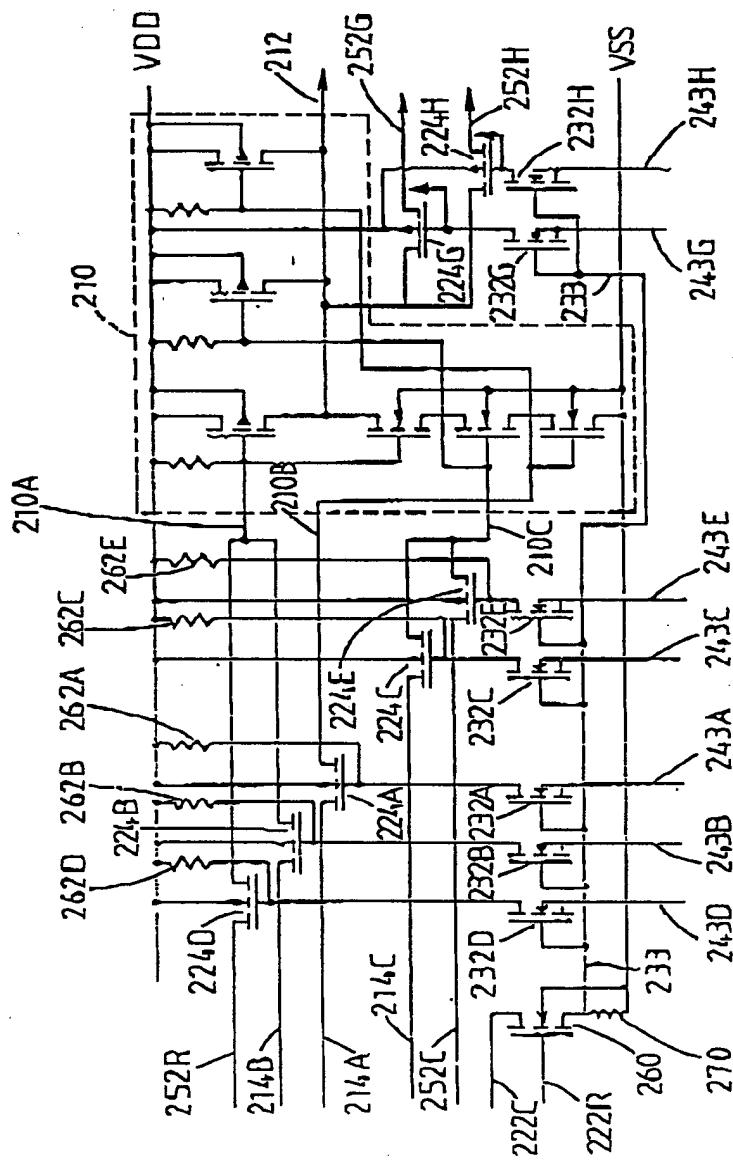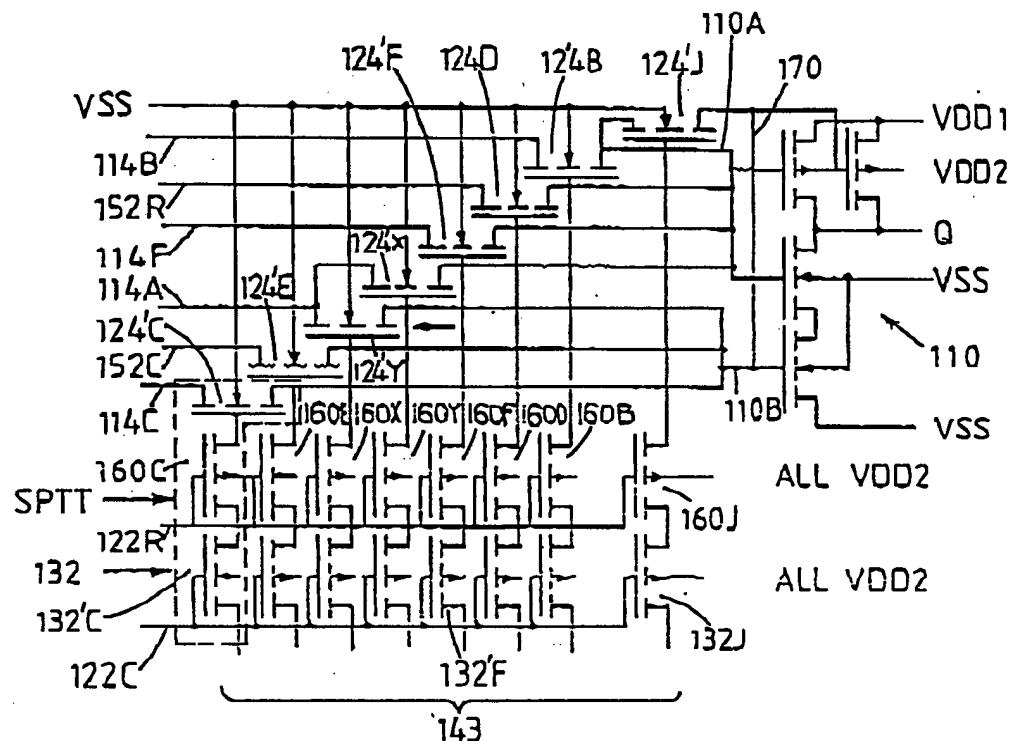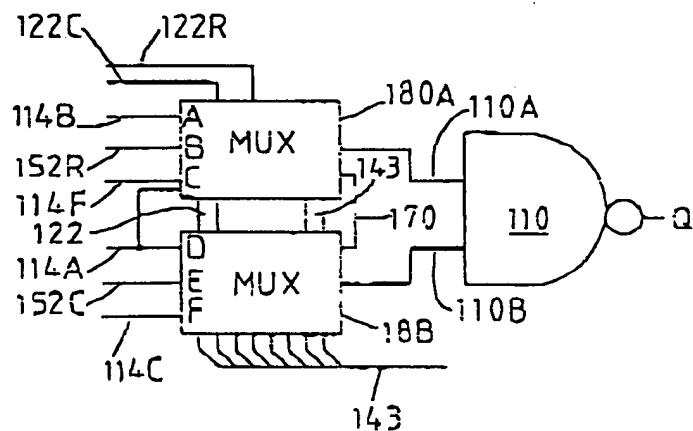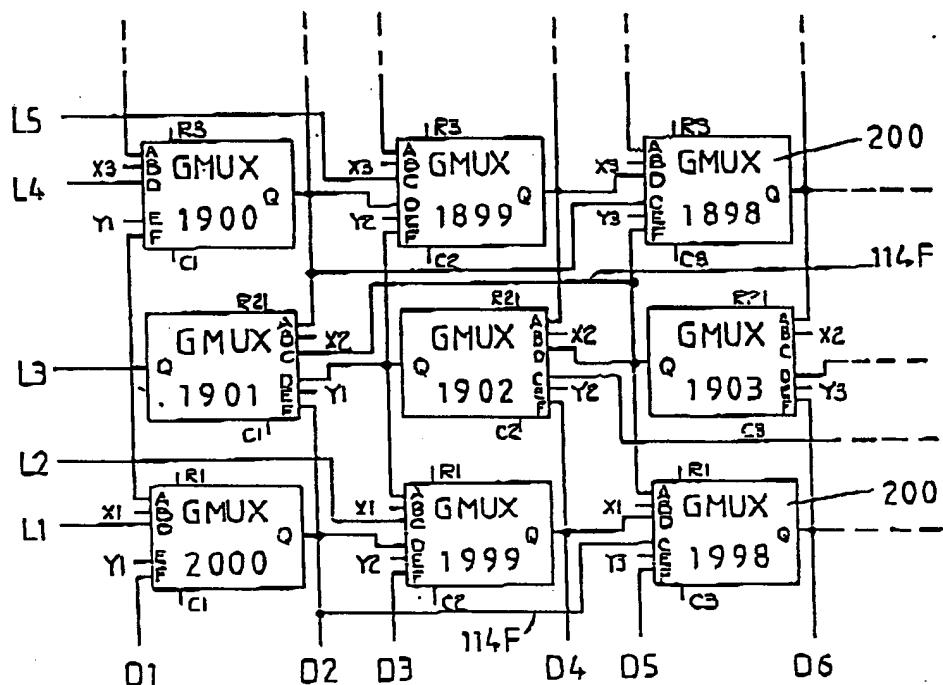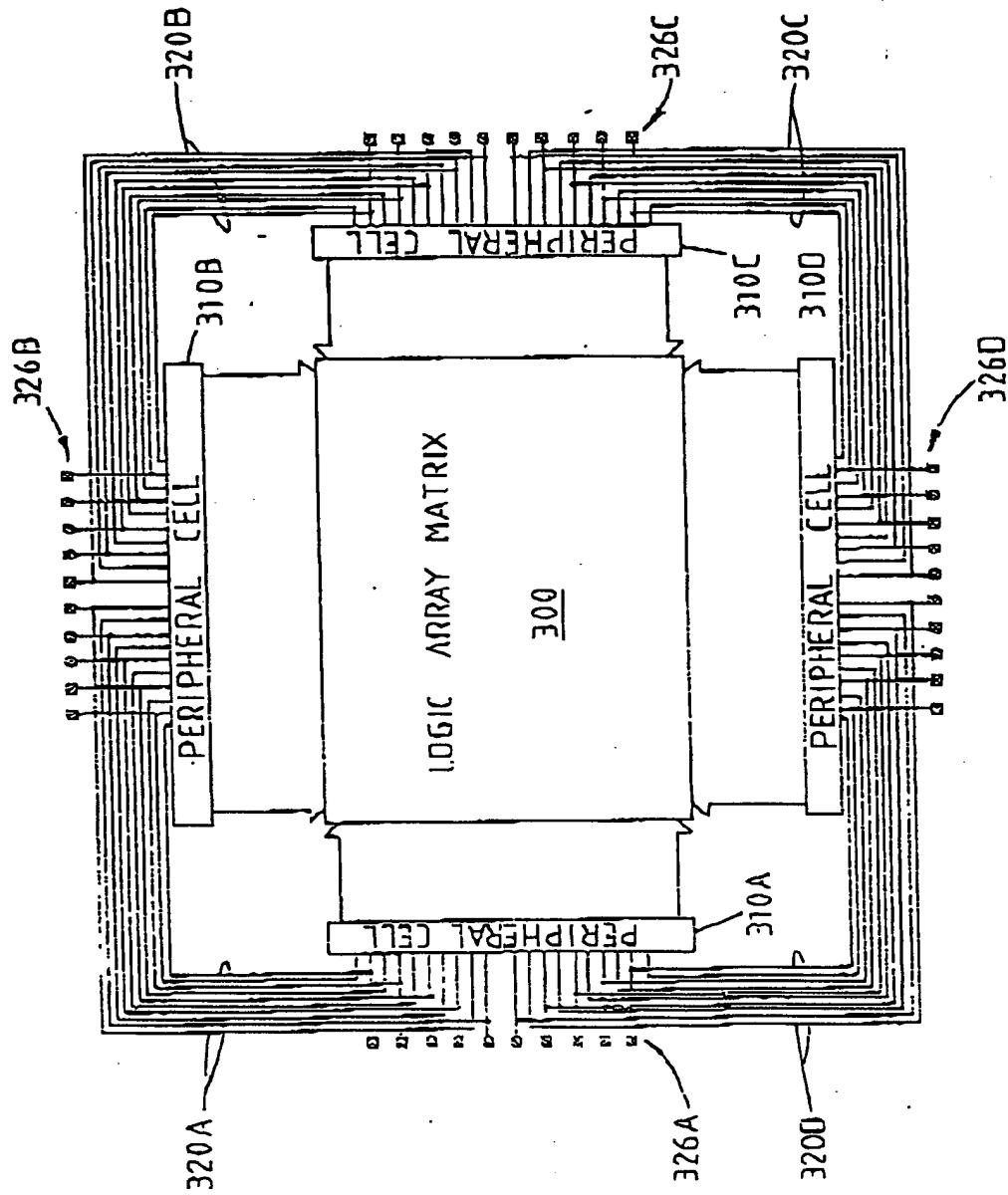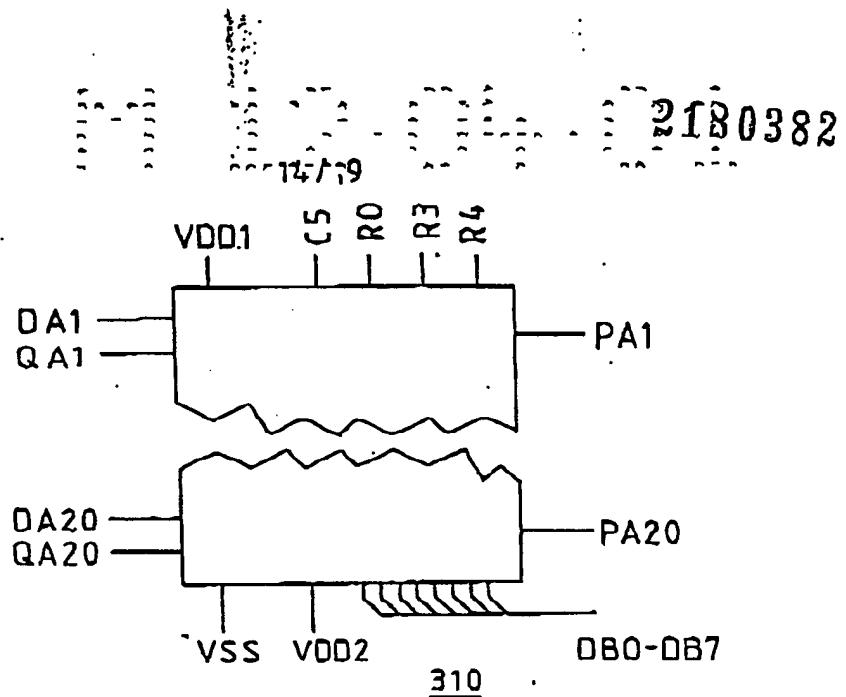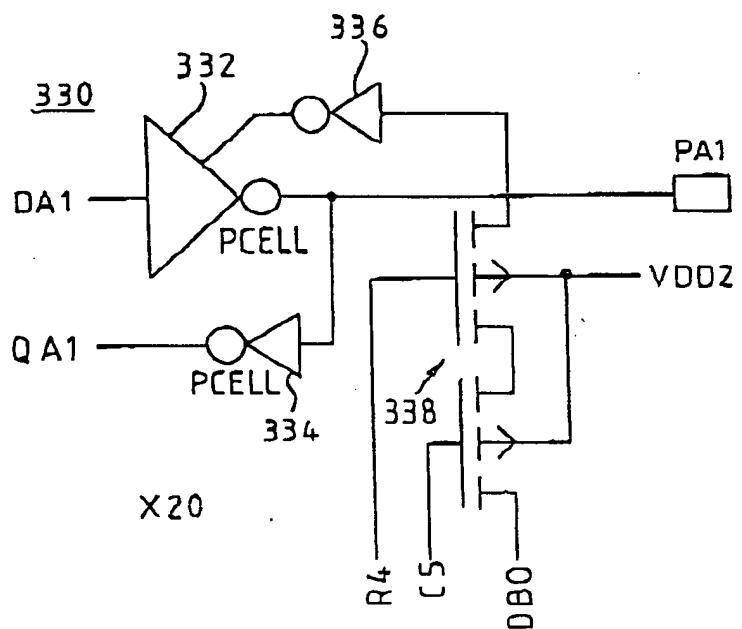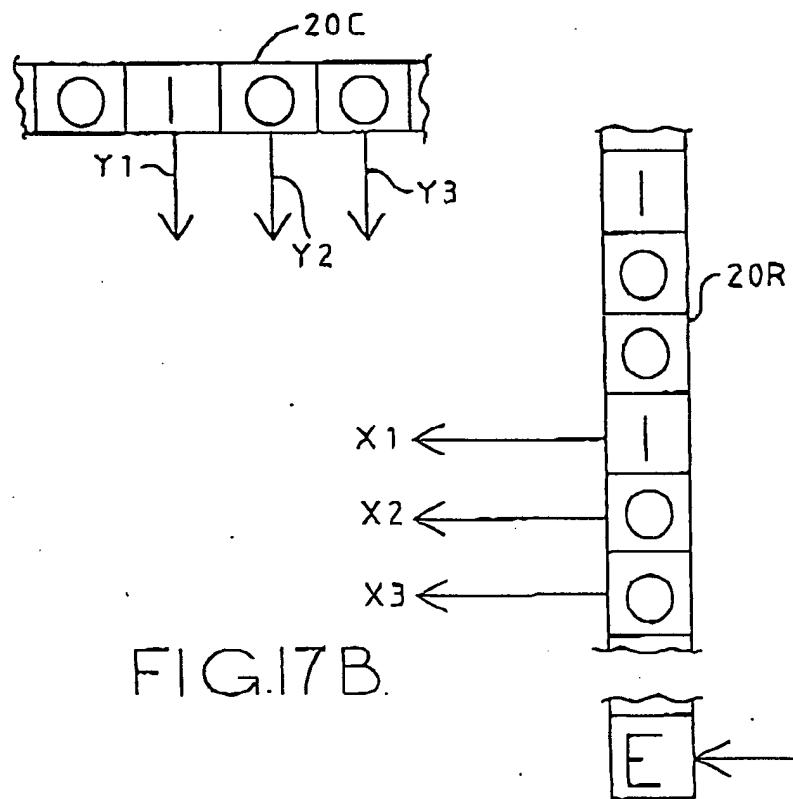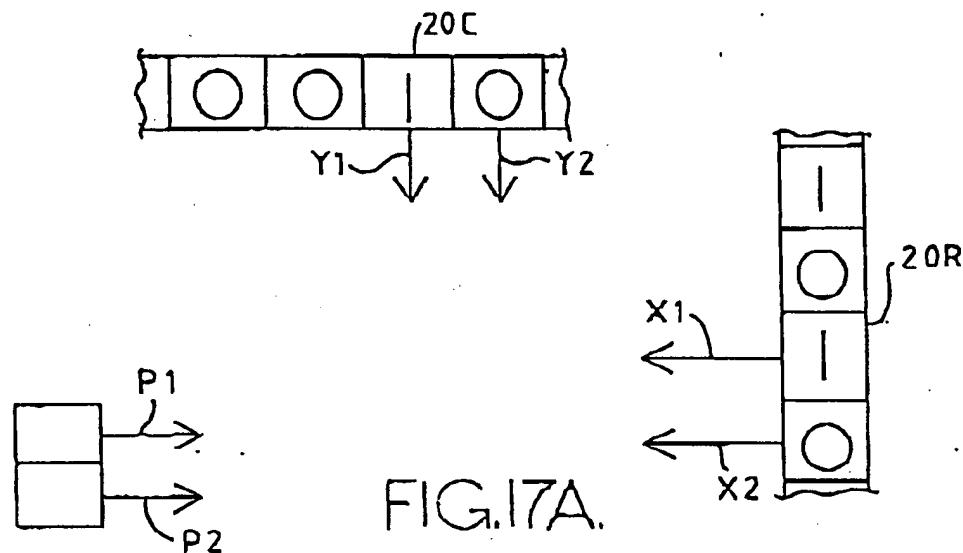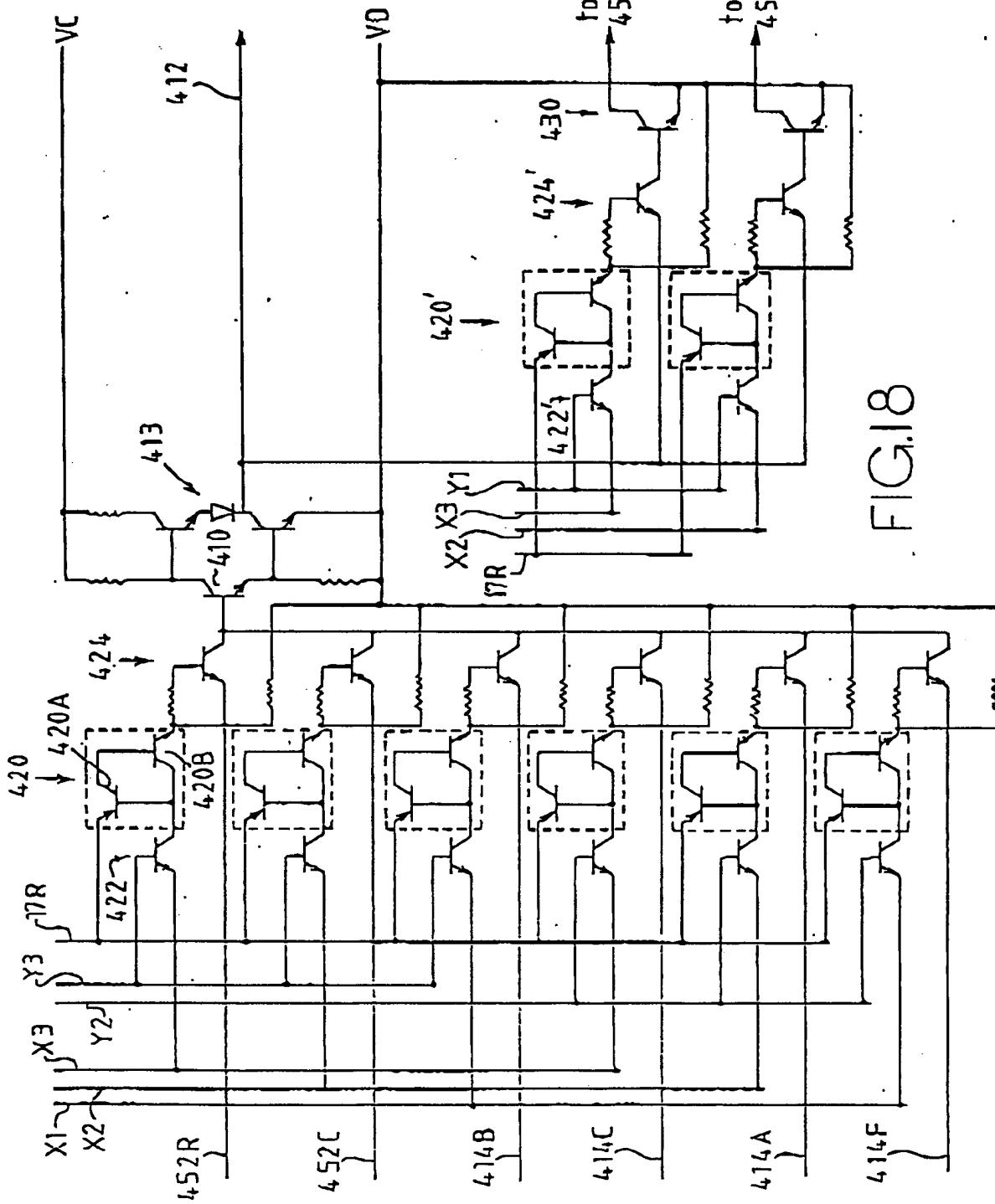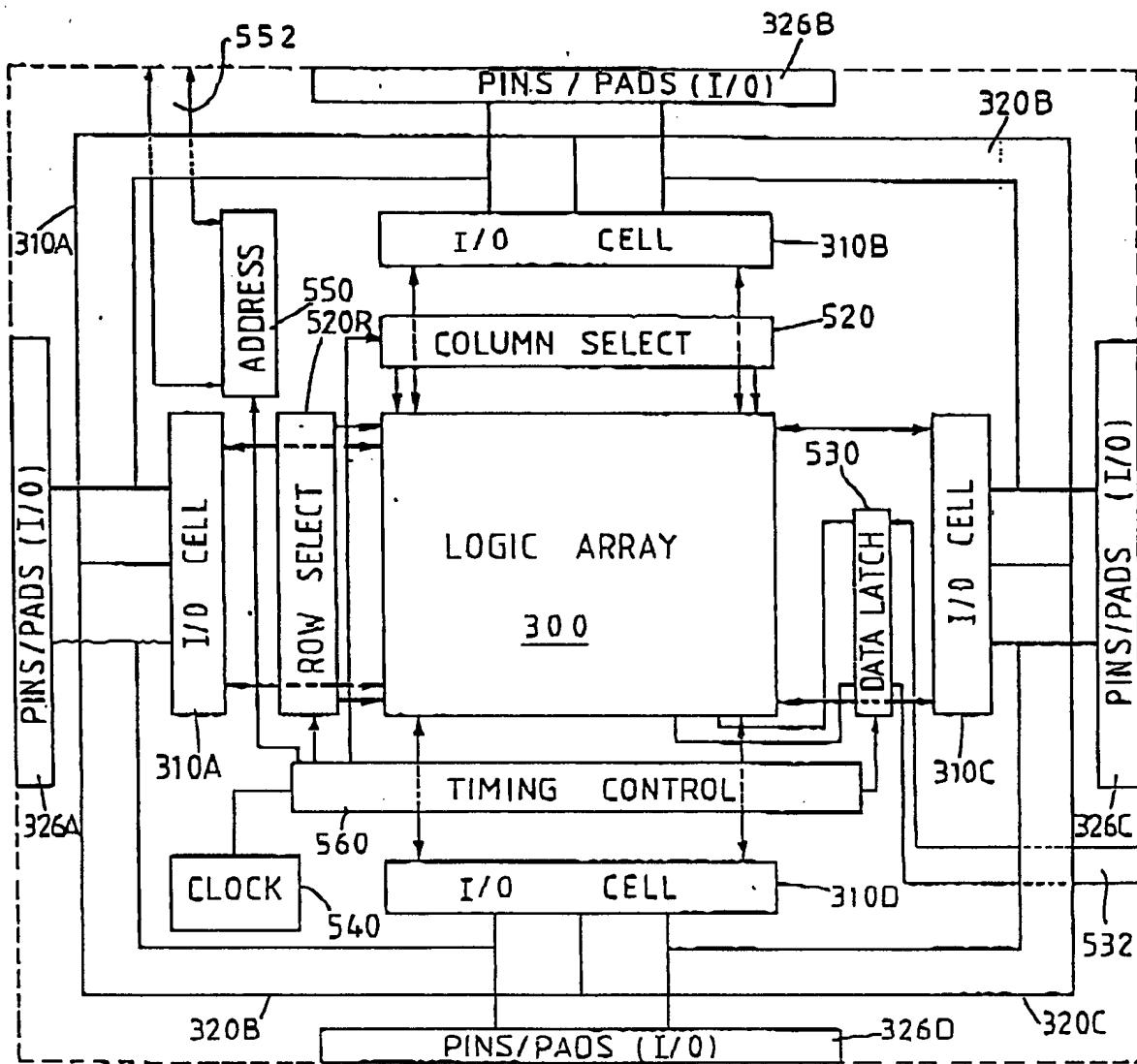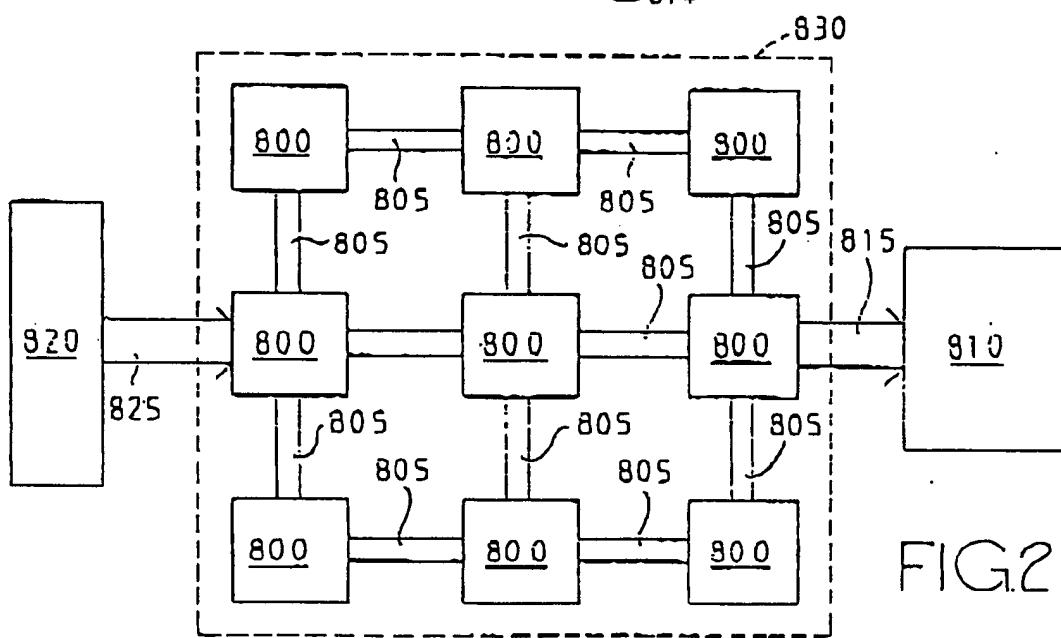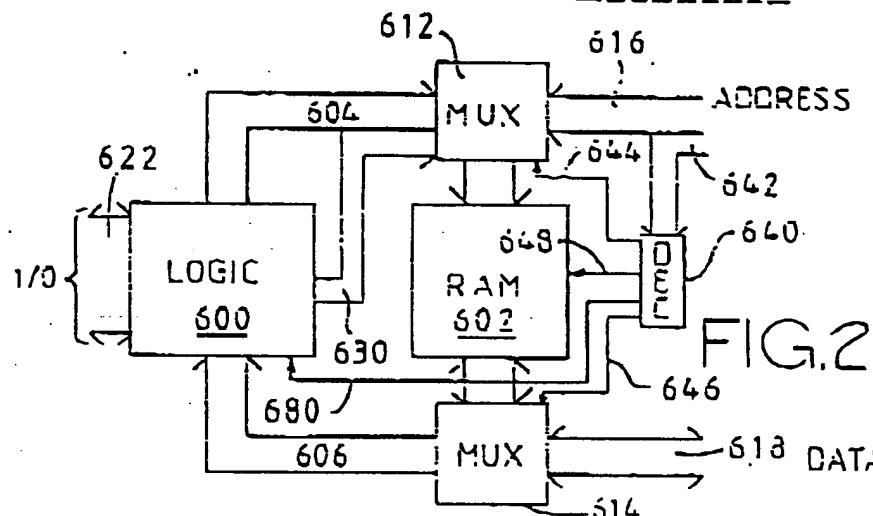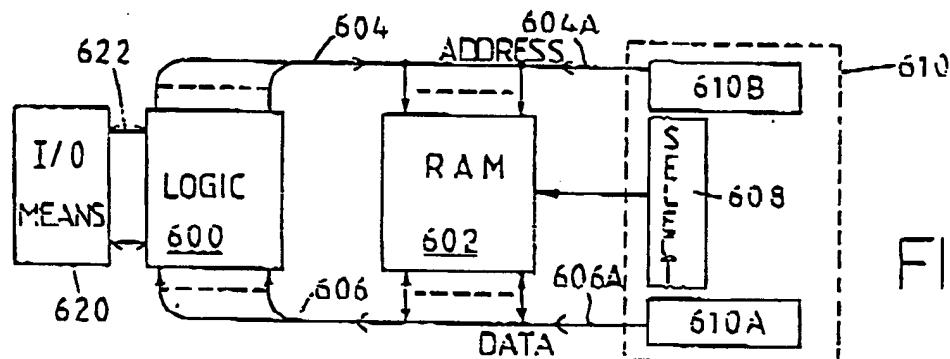
FIG.23.
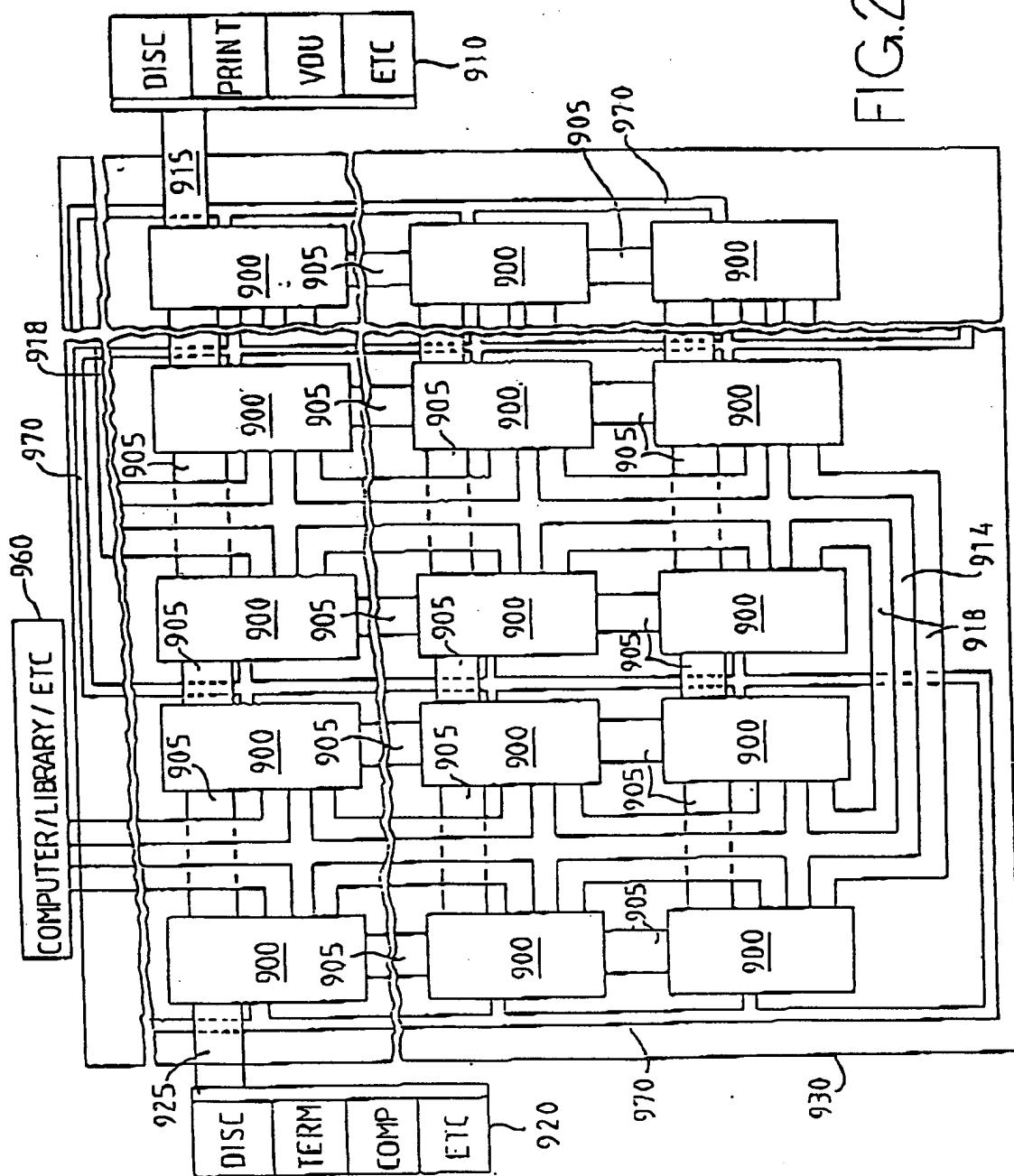
SPECIFICATION

Semiconductor Integrated circuits/systems

5 This invention relates to semiconductor electronic integrated circuits (chips) of the type comprising configurable logic circuit arrays, and systems utilising them.

Two types of such circuits are available at
10 present. One type is the so-called uncommitted logic array (ULA) in which a chip is first made with unconnected logic gates, i.e. each isolated at its own site on the chip, and interconnection for particular purposes is
15 achieved by means of a specially configured metallisation layer applied later. Usually, the gate sites are substantially uniformly distributed over the usable area of the chip or at least a central part of such area. Currently,
20 ULAs are available with from 500 to 5000 gates available and will doubtless increase in gate capacity as technology develops. Typically, around 60%-80% of available gates are utilised after interconnection to configure a
25 ULA for a particular purpose, it being in the nature of electronic circuit/system design that various local configurations of interconnected gates perform particular functions and are further interconnected for overall circuit/system
30 requirements, leaving some gates unused. Designing masks for such customised metallisation layers is time-consuming and expensive. Also, it is highly intolerant of errors as remasking is necessary whenever proto-
35 types malfunction by reason of design fault.

The other type is the so-called programmable gate array (PGA) in which a chip is formed with logic gates of which all or most are each individually interconnected with all or most of
40 the others in most if not all conceivable ways. The PGA as made is configured by fusing out unwanted ones of the interconnections. Usually, the gates are formed at edges of the usable area of the chip or that part dedicated
45 to PGA gate purposes, and a more central part of such area is occupied by a grid of interconnections fusible at crossing points or connecting devices. Not surprisingly, gate capacities are very much lower than for ULA's.
50 often effectively about 50 gates or less in terms of inclusion in actual logic functions. The capability of PGA's in terms of putting complex electronic circuit/systems into integrated circuit form is correspondingly limited
55 compared with ULA's. However, PGA's do have a very considerable advantage to the circuit designer, who need only take up another chip and start again whenever an error is made or malfunction is encountered requiring
60 re-design.

It would manifestly be of great advantage and practical utility to have configurable integrated circuits with greater gate capacity than such PGA's (say at least an order of magni-
65 tude greater if not approaching the gate capa-

cities of ULAs), but retain the ease of designer-use and freedom from masking-up costs that characterise PGAs compared with ULAs. It is towards providing such semicon-
70 ductor integrated circuits that this invention first directs its attention.

Several aspects of this invention arise in relation to the teaching hereof, and one aspect can be viewed as starting from questioning
75 the hitherto-accepted practice in relation to PGAs for all gate interconnection possibilities to be provided asmade and before configuration.

According to that aspect of this invention, a
80 configurable semiconductor integrated circuit (chip) as-made has formed therein a plurality of logic circuits at discrete sites and a restricted signal translation system between inputs and outputs of said logic circuits afford-
85 ing direct connection paths between each of said logic circuits and only a few others of said logic circuits, which connection paths are selectable as to their conduction state. Indirect connections to further of said logic circuits are
90 available through one or more others of said other logic circuits.

Suitable said selectable connection paths extend, for each logic circuit, from output thereof to inputs of a first set of others of
95 said logic circuits, and to inputs thereof from outputs of a second set of others of said logic circuits, all of the sets (for all of the logic circuits) each being unique. Normally, first and second sets associated with a parti-
100 cular logic circuit will have at least one said other logic circuit in common and most often at least one each not in common. Generally, each set will usually be a small proportion, less than 5%, of the total number of logic
105 circuits. It is envisaged that in many embodiments the number of logic circuits in a set will be 10 or less. Conveniently, the number in a set may be as small as five, but at least three except at edges of an array.
110 The term "as-made" as used herein means the chip (or some part thereof) in the state in which it is manufactured and prior to any operation to effect configuration. The term "selectable" as used herein in relation to a con-
115 nection path comprehends that the condition of the path as to whether or not it conducts in order to transmit electrical signals can be determined relative to its as-made condition by application of appropriate selection signals
120 or signal conditions. The term "logic circuit" as used herein is not intended to be restricted to the single function logic gates (such as NAND) used in illustrated embodiments, in fact could cover any logic circuit whose use with
125 interconnect provisions hereof proves to be feasible.

The direct connection paths are normally between physically neighbouring logic circuit sites, which, whilst not essential, facilitates
130 establishment of a desired particular circuit

function in a localised configuration of logic
circuits, i.e. in part only of the chip area occu-
pied by an appropriate number of discrete
sites of the logic circuits and by the direct
5 connection paths. Interconnections between
such localised configurations for overall circu-
it/system requirements can be either simply
by said direct connection paths or by said
indirect connections through selected ones of
10 the logic circuits. The inclusion of one or
more logic circuit transit times in some actual
configured indirect connections is usually of
small significance as such need not exceed
about 3 nanoseconds on present-day techno-
15 logy, at least for simple logic gate circuits.

We shall describe conduction selection pro-
visions for the direct connection paths at in-
puts to the logic circuit sites, i.e. in relation to
said second set of paths as entering the site.
20 However, they could equally well be provided
elsewhere, for example at logic circuit outputs,
particularly in branches therefrom (i.e. in rela-
tion to said first set of paths as leaving the
site). or at combinations of inputs and outputs
25 of logic circuit sites.

Concerning said direct connection paths and
appropriate physical dispositions of logic cir-
cuit sites on a chip, it is convenient to con-
sider matters in logic diagram terms correlat-
30 ing each logic circuit site as viewed on the
surface of a chip of semiconductor material
with a logic circuit symbol. The symbols/sites
will usually be arranged in an overall disposi-
tion of discernable regularity or pattern with
35 spaces between those logic circuit symbols/-
sites carrying said direct connection paths.
Examples of such regularity or pattern are ma-
trix arrays though there may well be offsets or
staggers of logic circuit sites in and/or be-
40 tween rows and/or columns. Such logic circu-
its may "point" in different directions
reflected on the area of the chip as sites be-
ing oppositely formed in terms of access to
inputs and outputs (or considering their out-
45 puts as establishing a direction after the man-
ner of an arrow-head). Several alternative dis-
positions of logic circuits, and their sites are
indicated with reference to the drawings, and
others may be equally or more efficient or
50 effective, at least in particular circumstances.

A presently preferred disposition in a basic
row-and-column, matrix-like, array, has each of
its logic circuits in each row "pointing" in one
direction and connected by a selectable con-
55 nection path from its output to input of the
next following logic circuit in the row. Further
preferably, such directions of successive rows
alternate thus making overall zig-zag or snake-
like indirect paths available throughout. Further
60 preferably, such logic circuit outputs are selec-
tably connected to inputs of the next adjacent
logic circuits in the same columns, i.e. those
in the next adjacent rows. That makes avail-
able paths running along columns, respec-
65 tively. Overall, such a disposition gives flexibil-

ity of selectable direct connections between
neighbouring logic circuits in a compact overall
arrangement of logic circuit sites. Such flexibil-
ity of interconnection is extendable in a parti-
70 cularly advantageous way by a further selecta-
ble direct connection path from output of each
logic circuit to input of the next-but-one logic
circuit in the same row going in the same
direction as the direct connection to the next
75 logic circuit.

The words "row" and "column" will usually
have some perceptible reflection in actual dis-
positions of logic circuit sites on a chip but
are used herein mainly for ease of explanation,
80 i.e. not for necessarily implying exactitude of
logic circuit site lay-out/topography. It should,
however, be clear that all embodiments of this
invention are intended to permit selection of
connection paths for configuration purposes
85 relative to logic circuit site dispositions that
can be substantially uniformly disposed over
at least part of the relevant area of a chip.

There is another aspect of this invention
concerning selectable connection provisions
90 traversing chip area of prime capability for for-
mation of logic circuit sites.

According to that aspect a configurable
semiconductor integrated circuit (chip) as-made
has a plurality of logic circuits formed therein
95 distributed over at least part of its usable
area, and a direct signal translation provision
comprising at least one conducting path asso-
ciated with selectable connection paths for in-
puts and outputs of said plurality of logic cir-
100 cuits or at least one subset thereof. Such path
or paths can be wholly or mainly in and along
spaces between discrete sites of said logic
circuits with selectable branch paths into
those sites. This provision is called herein a
105 direct connect bus system whose paths tra-
verse more of the logic gate sites than can be
reached by the first-discussed direct connec-
tion paths.

Whilst obviously applicable alone, this as-
110 pect has particular advantage when employed
in conjunction with the direct connection paths
of said restricted signal translation system in
order to provide selectable other direct con-
nections between non-neighbouring logic cir-
115 cuit sites. Such provision avoids logic circuit
transit times of said indirect connections and
allows direct connections between groups of
sites in different regions of said area. Dedi-
cated such other conducting paths can extend
120 along rows and columns of a matrix array of
logic circuits. Branches to two dedicated in-
puts at each logic circuit site can then be
selectable, as can further preferred branches
from each logic circuit output. Connections by
125 way of such direct connect bus connection
paths can go along selected rows or columns
and from one to another thereof in any de-
sired way, including providing disconnected
segments. It is not necessary for the conduct-
130 ing paths of such a direct connect bus system

all to be metallised as at least parts may be
paths through host semiconductor material of
enhanced conductivity, for example polysilicon
for silicon host material. Also, neither direction
5 of row and column conducting paths need ex-
tend continuously over the whole array of
logic circuit sites. They can be confined to a
subset of the logic gates of the array, or be
be provided localised to each of several sub-
10 sets. Any necessary further interconnection
relative to the subsets can be through a logic
circuit or circuits.
It can be advantageous for segmented sec-
tions of such paths, which may correspond to
15 different subsets, to overlap each other by at
least one logic circuit site. Segmented pro-
visions are particularly useful for conductivity-
enhanced paths or parts of paths as they
should then be of limited extent, say up to six
20 logic circuit sites, in view of their greater im-
pedance compared with metallised paths. For
example, the row-following paths could be
metallised, perhaps interrupted once with pos-
sible interconnection through a logic circuit,
25 whilst the column-following paths could be of
polysilicon in much shorter interleaved and
overlapped lengths and also interconnectable
by means of logic circuits.
It is found convenient for all selection pro-
30 visions of input connection paths to a particu-
lar logic circuit, and any selection provisions
of output connection paths therefrom, to be
adjacent to that particular logic circuit, and
thus be considered as included in the logic
35 circuit site.
To provide for selective addressing of logic
circuit sites, (in relation to configuring selecta-
ble connection paths to their inputs or from
their outputs), spaces between them can be
40 further traversed by specific row and column
extending conducting paths (address paths).
The latter conveniently enter the site of each
logic circuit through branches from each of
corrresponding row and column address
45 paths, and have associated further circuitry to
serve in affording (by coincident energisation)
circuit conditions contributing to selection of
required selectable connection paths, for
example establishing voltage levels assuring
50 required response to an actual configuring sig-
nal.
For configuring addressed logic circuits in
relation to their selectable and desired connec-
tion paths, it is further an aspect hereof that a
55 configuring (program) bus system is provided
having a number of (program) conducting
paths corresponding to the maximum number
of selectable connection paths in any of the
logic circuit sites. The program conducting
60 paths traverse (usually between but branched
into) all of the logic circuit sites and operate
at least to complete circuit conditions required
for configuration, usually to deliver configuring
electrical signals.
65 Then, the address paths can condition all of

the selectable paths at logic circuit sites as
selected sequentially, and, at each site in turn,
the program paths cooperate to effect the re-
quired configuration by changing the conduc-
70 tion state of appropriate selectable connection
paths. For the purposes of selectability, circuit
elements are provided, one per selectable con-
nection path, and the as-made conduction
state of those circuit elements can be changed
75 by a said configuring electrical signal or circuit
condition.
An alternative is for more address paths to
go to each logic circuit site and to have
coded connections relative to the selectable
80 connection paths at that site so as sequenti-
ally to achieve at least conditioning of a differ-
ent one or more (less than all) of the selecta-
ble connection paths.
That leads to provision of two or more of
85 each of row and column address paths, but to
a reduction in the number of program paths
required. Each of the reduced number of pro-
gram paths will service more than one of the
selectable connection paths at each logic cir-
90 cuit site but only one of them will be condi-
tioned at any one time by the address paths.
Where there are enough address paths to
identify each selectable connection path at
each site, the program paths could be re-
95 placed by a single configuring signal path,
otherwise enabling of address path energisa-
tion could be on a selective basis if such en-
ergisation is enough also to achieve circuit
conditions causing configuration automatically.
100 At least where the circuit elements of the
selectable connection paths are normally con-
ducting in the chip as-made, and to be ren-
dered irreversibly non-conducting, they can
comprise what we call conducting links,
105 whether of fusible conductor or of other disa-
blable type (say a diode to be "blown"). As-
sociated further circuitry will normally include
an active circuit device conditioned to pass a
disabling electric current as a said configuring
110 signal. Otherwise, blocking signals might be
used for controlling current steering means (of
said further circuitry) by which disabling cur-
rent flow will otherwise be applied to each of
those circuit elements of the addressed logic
115 circuit site whose steering means is not
blocked.
An alternative to fusible or otherwise irre-
versibly disabled conducting links comprises
switchably conducting/non-conducting circuit
120 elements, typically active circuit components,
for example transistors. Then, signals on the
address and program paths, or coded address
paths only, can be used to provide suitable
conditions for setting the reversible conduction
125 state of those circuit elements. Typically, ac-
tive circuit devices (for example also transis-
tors) of associated further circuitry are in suit-
able circuit configuration with the selectably
conducting/non-conducting circuit elements to
130 condition the latter for conduction. Some em-

bodiments of this invention will have configured conduction states that, in operation, remain until reconfigured (static) and other embodiments will require refreshing of their confi-
5 gured conduction states (dynamic).

For CMOS integrated circuit technology, chargetrapping transistors, for example floating gate transistors or oxide-nitride sandwich transistors, can set up selected conduction states
10 that are static for associated selectable connection paths in a manner somewhat analagous to that used in relation to EPROMs. Here, though, such charge-trapping transistors are used to control circuit elements comprising
15 normal MOS transistors, specifically to determine whether those MOS transistors are to be conductive as selectively configured.

An alternative would be to establish such control conditions by way of combinations of
20 MOS transistors and capacitors in a manner analagous to that used in relation to so-called dynamic read/write memories (DRAMS), but then, of course, requiring refreshing, i.e. on a dynamic basis.
25 A significant development concerning use of single signal-pass field-effect transistors as selectable connection-controlling circuit elements is the subject of another patent application.

Basically, in a field effect semiconductor
30 chip, a single signal-pass transistor is connected between bit signal input and bit signal output and has its control electrode connected for temporary energisations by switching circuitry operative only at prescribed intervals,
35 the single signal-pass transistor being operative to pass signals between such energisations of its control electrode. Those energisations render the single signal-pass transistor conductive, i.e. enabled for conduction, and
40 that conduction is caused to persist, though with some decay, hence periodic refreshing at said prescribed intervals. Inherent capacitance of the single signal-pass transistor inevitably results in accumulation of charge during each
45 said energisation applied to its control electrode. The switching circuitry operates, not to apply discharge voltage between such energisations at said prescribed intervals, but rather to leave the control electrode "floating" be-
50 tween refreshes by said energisations. Such single signal-pass transistors are, of course, capable of continuous signal passage despite only intermittent energisation of their control electrodes.
55 We further propose an alternative single signal-pass transistor for bipolar semiconductor chips, which will also operate at or near normal logic voltage levels and speeds, and do so without requiring refreshing. That proposal
60 involves circuit formations resembling, at least in action, a silicon-controlled-rectifier (SCR) associated with another transistor for selection to condition for triggering that will force the single signal pass transistor into conduction
65 until reset or loss of power supply. At least

for a NAND gate, the signal-pass transistor can effectively be an input stage of the gate.

It should be evident that envisaged alternatives to irreversibly fusible or disabled links or
70 parts, indeed all feasible reversible conduction schemes/devices lead to integrated circuits of this invention that are reconfigurable.

Amongst important implications is the possibility of re-using the same chip, whether by a
75 designer in prototyping or developing a particular system/function, or by a manufacturer to adjust his inventory. Chips employing charge-trapping transistors could be reconfigured by suitable equipment, for example an EpROM
80 writer, whether working from a model or master chip or from the contents of some store that could be part of a programmed computer system serving as a design terminal and/or library of available configurations. Any such
85 applied configuration will be static, i.e. not require refreshing, but configuration will usually be much slower and require much higher signal levels than applies to its subsequent operation as a configured logic system. That
90 would militate against reconfiguration in actual use, though EEpROM chip development may make that feasible.

However, there is the possibility of reconfiguring at or near normal logic signal levels and
95 speeds, which would apply to the afore-mentioned chips using DRAM- type MOS transistor/capacitor combinations, and is yet more efficiently achieved by our single signal pass transistor proposals. Such chips of field effect
100 type are generally of a dynamic nature requiring refreshing of any resident configuration, but bipolar chips can be of a static nature using our SCR-related proposal.

Reconfigurability underlies other aspects of
105 this invention, i.e. regardless of whether the reconfigurable chips are as envisaged herein or whether they are of some other design and implementation.

According to such an aspect of this inven-
110 tion an electronic system utilising a reconfigurable chip further comprises means for presenting to that chip, whenever configuration is required, electrical input signals defining the then-desired configuration. Such electronic
115 systems will normally be digital, and can include means for utilising signals from the chip, preferably also means for presenting signals to the chip.

Defining signals may be presented according
120 to the contents of a store system, whether permanent or semi-permanent or temporary according to the state of a computer or other data processing system. However, any source of defining signals can be used.
125 Using one or more reconfigurable chips, at least a part of an overall electronic system can have a reconfiguration capability, whether as alternative back-up configurations for one or more particular functions, or as alternative
130 functions not required together, or some com-

binaton of both. For alternative functions the
presenting means may include a sequencer, ;
say in association with appropriate store sys-
tem addressing means. parts of chips hereof
5 might well be configured as addressing means
to serve in successive reconfigurations
thereof, especially from a specific associated
store, preferably a RAM.
Reconfiguring of chips at or near normal
10 logic signal levels and speeds could provide
an electronic system with fewer chips because
at least some of them can be reconfigured to
take on a sequence of at least two functions
that would otherwise require separate chips
15 but whose functions are not actually required
simultaneously. Also, any desired number of
reconfigurable chips can be configured to-
gether for desired serial processing, or to per-
form parallel processing. The latter could be
20 on parts of the same algorithm or function,
say with different start points of a spectrum
of data for investigation by that algorithm or
function, thereby effectively multiplying the
rate of operations performed per unit of time.
25 Such systems may conveniently have reconfi-
gurable chips on the same printed circuit
board also having address/data bus systems.
Each chip can have a store, usually RAM as-
sociated therewith. The data proceeding
30 power of such a system can be very high for
very low cost.
At least where any one chip to be confi-
gured essentially to a particular purpose is
capable of alternative possible configurations
35 to the same purpose, i.e. for reconfiguration in
the event of failure of the current configura-
tion, same may be done on an automatic ba-
sis according to results of test procedures/-
functions that may be externally applied and
40 controlled or. advantageously, incorporated
onto the chip concerned or at least its associ-
ated store.
At least in connection with reconfigurable
chips, it has been found advantageous to
45 make special provisions on the chips regarding
input/output. Various features thereof include:
(a) providing, for edge-most configurable
logic circuit sites, input/output circuitry as per-
ipheral cells that afford multiple access be-
50 tween actual edge pins or pads for input/out-
put signals and a greater number or input/out-
put lines of the edge-most logic circuit sites,
preferably both to one input of each edge-
most logic circuit site and from its output,
55 though it is advantageous for each of the lat-
ter to serve a dual purpose in being further
connected to inputs of the next in-array ones
of the logic circuit sites;
(b) providing that at least some individual
60 subcells of such peripheral cells are configura-
ble and reconfigurable to serve input or output
purposes, conveniently correlated at least with
lines that can serve as output from edge-most
logic circuit sites and input to next edge-most
65 logic circuit sites, and preferably further af-

fording signal transmission from and back to
the logic circuit sites;
(c) providing for multiple connections of in-
put/output lines of logic circuit sites to sub-
70 cells on an efficient and orderly basis;
(d) providing a peripheral cell of such sub-
cells on each of at least two sides, preferably
all four, of a physically rectangular array of
logic circuit sites;
75 (e) providing side-wise extending conducting
paths outside peripheral cells which paths af-
ford alternative connections from edge pins or
pads to peripheral cells at adjacent sides.
It may well be that other features or combi-
80 nations of features will prove to be both novel
and useful, in which case same are further to
be considered as inventive aspects.
Specific implementation of this invention will
now be described, by way of example, with
85 reference to the accompanying diagrammatic
drawings, in which:
Figure 1 shows a basic logic circuit array
layout. actually of NAND gates;
Figure 2 shows a variant gate layout with
90 an extra direct gate connection;
Figure 3 diagrammatically adds to Figure 1 a
addressing conduction path layout;
Figure 4 diagrammatically adds to Figure 1 a
program bus system layout;
95 Figure 5 diagrammatically adds to Figure 1 a
direct connect bus system layout;
Figure 6 shows a variant direct connect bus
system segmented for subsets of the gate ar-
ray. and
100 Figure 6A shows a modification;
Figure 7 is a diagram showing all of the
Figures 3. 4 and 5 provisons on twelve logic
circuits of the Figure 2 layout.
Figure 8 is a circuit diagram of a NAND gate
105 site using fusible links for its configuration;
Figure 9 is a circuit diagram of a two-input
NAND gate site using reconfigurable connec-
tions of static MOS type;
Figure 10 is a circuit diagram for a three-
110 input NAND gate side on a similar basis to
Figure 9;
Figure 11 is a circuit diagram relating to a
NAND gate site using reconfigurable connec-
tions of a dynamic MOS type;
115 Figure 12 is a block circuit representation of
the Figure 13 embodiment;
Figure 13 is a block circuit diagram of Fig-
ure 12 gate sites at a corner of a reconfigura-
ble array;
120 Figure 14 is a schematic diagram of a re-
configurable gate array (300) and peripheral in-
put/output cells (310A, B, C, D);
Figure 15 is a block circuit representation of
a peripheral cell;
125 Figure 16 is a schematic circuit diagram of a
typical subcell of the peripheral cell;
Figures 17A and 17B show variant selection
logic;
Figure 18 is a circuit diagram of a NAND
130 gate site using bipolar technology and reconfi-

gurable without requiring refreshment;

Figure 19 gives an indication of what will normally be present on a chip hereof;

Figures 20 to 22 are block circuit diagrams
5 useful in explaining systems applications of chips hereof; and .

Figure 23 shows how a plural chip system can be implemented on a printed circuit board.

In the drawings, we show NAND gates as
10 the aforesaid logic circuits, but that should not be taken as limiting.

Referring first to Figure 1, a semiconductor chip as-made will have an area thereof carrying a matrix array of NAND gates 10 at dis-
15 crete sites. For clarity of illustration, the matrix array as shown is small compared with a normal actual layout, which can extend to thousands of gate sites. As-made, the chip also has direct gate connection paths 14. For each
20 gate in rows and columns other than those at edges, its output 12 is directly connected at 14A to input of the next gate in nose-to-tail serial fashion along rows. Output 12 is further connected at 14B, 14C to inputs of gates that
25 with its gates disposed nose-to-tail serially in the opposite direction. Each of the direct connection paths 14A, B, C is of conduction-selectable type. Gates at ends of rows and columns have direct connection paths so far de-
30 scribed, and unused connection paths can serve for data input and output for the array of gates.

Figure 2 shows the same basic gate array layout connection of its output to input of the
35 next but one gate in its row, shown as selectable connection path 14F.

Considering each gate as directly connected by other gates, and by paths between its inputs and outputs of a second set of other
40 gates, no gate has less than one other gate in common between those sets, and at least one other gate not common. In fact, in Figures 1 and 2, all but those at edges of the array gates have at least three gates in each of its
45 sets, of which two are common to both sets and one (Figure 1) or two (Figure 2) of each set are not. The common gates actually share the same column as the gate concerned and the others share the same row. First (FS) and
50 second (SS) sets are shown for one gate (10R) in Figures 1 and 2.

The arrangement of Figure 1 is particularly compact, and is readily implemented using one metallisation layer. The enhancement of
55 Figure 2 is powerful in extending the flexibility of direct connection selection in arriving at logic-function-performing interconnections of gates on a local basis, but does require "crossovers". As applies throughout this descrip-
60 tion, "crossovers" can be obtained by more than one metallisation, or by appropriate combination of metallisation and conductivity-enhanced semiconductor material, say polysilicon for silicon chips.
65 Alternative enhancements of the direct con-

nection paths of Figure 1. could involve direct connection paths from each gate output to input of a gate in the next column but next-but-one row. That generally involves one less
70 cross-over than Figure 2 but is obviously less powerful in going along rows where the "hopping" effect of the Figure 2 layout is particularly effective. Direct connection of gate outputs to inputs of the next gate in the same
75 row is considered particularly powerful, but may not always be essential. Another possibility has other direct connection paths going to gates in next adjacent rows but the next column. mainly to get improved diagonal inter-
80 connections over the chip.

Alternative dispositions of gates include adjacent pairs of rows "pointing" in one direction but adjacent pairs "pointing" in opposite directions. One direct connection path scheme
85 again had gate outputs connected to input of the next gate in the same row, and two other direct connections to the next but one gates in the same column. That made logic function interconnections of gates less localised in
90 themselves, though they can be at least partly interleaved as the overall gate layout resembles two diagonally offset or intercalated layouts of Figure 1. An alternative for the same gate layout is for gate outputs to be
95 connected to inputs of next gates in the same column, giving alternate encouragement of different directions of interconnection.

At least for certain types of logic function design, other gate layouts can be with not all
100 gates in the same direction in each row, and can use other provisions of selectable direct connections.

It will be appreciated from the foregoing, that local direct connection paths (14A, B, C,
105 F) do allow for indirect connections between different parts of the array of gates 10 on the basis of selective traversal of gates 10 then acting simply as inverters, i.e. with their other connections non-conducting. Such use of
110 gates in indirect connections does not normally represent any significant reduction of gate utilisation relative to ULAs as the latter normally use only 60%-80% of gate capacity, and the unused gates are inevitably normally
115 close to and between parts of the array configured, respectively, to perform particular constituent functions or subfunctions.

However, referring to Figure 5, it is the case that the preferred embodiments hereof further
120 include another signal translation system, by way of a direct connect bus directly connected to gates 10 throughout the array. That is done using a grid of other connecting paths, see row and column conductors 50R,
125 50C going to each gate site in the corresponding row or column thereof. They utilise (Figure 7) other dedicated selectable connection paths, shown as inputs 14D, 14E of the gate sites 10S (or gates 10 in Figure 8), (from
130 branches 52R, 52C of such conductors 50R,

50C. In addition (Figure 7), output 12 of each gate 10 can be branched at 52G, 52H back to the conductors 50R, 50C and that will then be through other selectable connection paths.

5   The direct connect bus system 50 does not have to be continuously coextensive with the entire area of the chip occupied by gates 10. Indeed, it is preferably not so where any part of row and/or column paths 50R, 50C are

10 through conductivity-enhanced semiconductor material rather than along metallisation. For silicon chips of 3-micron MOS type, it is found advisable not to have extents of polysilicon beyond that required to traverse six row or

15 column gates.

Figure 6 shows a direct connect bus system that is effectively as Figure 5 but segmented into quadrant subsets 50A-D. Constituent conducting paths are shown (at 51A-D) individu-

20 ally interconnected one-to-one by selectable circuit elements that may be fusible conducting links or selectively enabled/disabled conduction devices such as transistors, see MOS transistors as indicated. It will be appreciated

25 that constituent conducting paths of one or more subsets can be extended into other subsets or not as required, also that there may be more or less subsets than the four shown. Moreover, a particularly convenient segmenting

30 arrangement is available through a modification shown in Figure 6A, wherein the connection means 51A-D are not shown and at least some paths (53A, 53B) of each subset are extended by at least one gate (10Z) beyond

35 their specific subset (10A, 10B) to give interleaved overlapping. Then, the necessary interconnections to extend each such path can be achieved through logic gates.

Shift registers 20R, 20C are shown in Figure

40 3 for sets of row and column following conducting address paths 22R, 22C each serving all the gate sites of its corresponding row or column. At crossing points, each row conductor 22R and each column conductor 22C have

45 branches entering the same gate site (see Figure 7 and 10X in Figure 3), so that they can be used in addressing on a coincident signal basis. Such addressing provides, at each addressed gate site an electrical circuit condition

50 required for configuring desired ones of all selectable connections at that site, say by way of enabling application of configuring electrical signals.

The purpose of the shift registers 20R, 20C

55 is, of course, to provide efficient sequential energisation of the gate array, say using a single input pin 30 via which all of the desired addressing contents for both registers is clocked, a single different binary value from

60 each then being sufficient to select any particular gate 10. One shift register could be further usable/extended to store "program" signals for deciding which selectable paths are required at any selected gate site, or a data

65 latch may be used.

In Figure 4, a program bus system 40 is indicated traversing all gates of the array in zig-zag or snake-like manner see end links 40A 40B. The program bus is branched into

70 every gate site (see 43 in Figure 7). In one arrangement, there is one line (see 42 in Figure 8) of the program bus dedicated to each different selectable connection of any gate site.

75 Figure 7 shows in-principle incorporation of the Figures 2 to 5 provisions relative to logic circuit sites 10S that could include NAND gate, or other logic function gates, indeed any useful logic circuitry or combination thereof.

80 The sites 10S each include all selectable circuitry provisions for the selectable direct connection paths 14 and for the branches from direct connect bus paths 50R, 50C.

One actual provision for selection of selecta-

85 ble connection paths at each gate 10 is indicated in Figure 8 by means of fusible conducting links 24, i.e. a static irreversibly configurable arrangement. Figure 8 shows a complete gate site together with traversing address

90 paths (22R,C), program paths (42), and power supply path 61. There, application of a configuring electrical signal as fusing current requires one of field effect transistors 32 (shown as n-channel MOS) formed on the chip

95 to be rendered conductive. Each transistor 32 has its gate electrode connected to the row select line 22R and an input electrode connected to the column select line 22C so as to conduct only when both such lines are ener-

100 gised. When that occurs it changes the voltage condition of line 33 from the transistor 32.

In order to complete circuit conditions for fusing current to flow, program bus lines 42

105 (of 40) are shown branched, see lines 43 extending therefrom and including steering diodes 34. The lines 33 and 43 are connected to each side of the links 24 in input lines 14 to the gate 10. At a gate site selected by

110 address lines 22R, 22C, all transistors 32 are enabled, but configuring circuit conditions further depend on energisation of the program lines. Fusing current will flow only through fusible links 24 for which program branches to

115 lines 43 are appropriately energised.

One other feature shown in Figure 8 is feed resistors 62 from power supply line 61 paralleling respective ones of the transistors 32 and serving for NAND gates 10 to hold dis-

120 abled gate inputs at an appropriate logic level. Obviously, a different voltage level and corresponding holding provision would apply for a NOR gate array.

It will be noted that gate inputs 14, fusible

125 connecting links 24, transistors 32, lines 33, diodes 34, program lines 42 and branches 43, are subscripted A, B, C, D, E, G, H to indicate their operation relative to direction connection paths (A, B, C) and direct connect bus bran-

130 ches (D, E to inputs, and G, H at output bran-

ches), respectively. Output branches to 52G, 52H are shown controlled from a single transistor 32G, but separate ones could be provided if desired.

5· It will be appreciated that Figure 8 shows gate site input selection, i.e. effectively relative to the second set (SS) of Figure 1. If preferred or desired, conducting link selection for the paths to inputs 14A, B, C could be pro-
10 vided at outputs from other sites of the other gate sites to which they afford selectable connection. Then outputs 12 would have branches serviced by fusible links, then effectively relative to the first set (FS) of Figure 1 at
15 each gate site.

The fusible conducting links 24 might be replaced by other selectable conducting links, such as diodes, to be disabled irreversibly (blown). If diodes are used instead of the fusi-
20· ble links 24, a parallel pair of oppositely poled diodes can be provided, one of which is blown. In other arrangements as described with reference to Figures 9,11, the selectability of the connection paths can be achieved
·25 by active circuit components, typically transistors which are included in the paths and the state of which, conducting or non-conducting, conditions the selectable connection path.

There are alternatives to providing a full pro-
30 gram bus 40. Thus, a coding for multiple energisation (say two at a time) of a number of paths or lines less than the number of links involved can be used to identify individual links one at a time at an addressed gate site.
35 That can be done without further requirement for logic at gate sites, by having more than one of each of the row and column lines 22R, 22C but having a unique pair of them connected to opposite sides of any one of the
40 transistor 33—line 24—diode 34 combinations.

Examples are given in Figures 17A and 17B. In Figure 17A, for each row and column of gate sites, there are two row address paths
45 X1, X2 and two column address paths Y1, Y2. There are also two program bus paths P1, P2 that go to all gate sites. Up to eight selectable connection paths can be serviced at each gate site. Each pair of row and column
50 address paths (Y1, X1; Y1, X2; Y2, X1; Y2, X2) will identify two selectable connection paths at the gate sites where they coincide, and the program paths P1 and P2 will serve in selectively applying configuring electrical
55 signals. In Figure 17B, there are three row address paths X1 X2 X3 and three column address paths Y1, Y2, Y3 going along each row and column of gate sites. They enable identification of up to nine selectable connec-
60 tion paths at a gate site, again on a coincident current basis (Y1, X1; Y1, X2; Y1, X3; Y2, X1; Y2, X2; Y2, X3; Y3, X1; Y3, X2; Y3, X3). Where configuring electrical signals are required, a single path for that purpose will
65 replace the above-discussed plural program

paths. If the selectable connection paths can respond directly and only to applied address signals (as will be described for Figure 18), only a selectively applied enable signal (ES) is
70 required for one of the sources of row and column address signals. In Figures 17A, 17B, such sources are again shown as shift registers 20B, 20C and will obviously be longer than required for single row/column address
75 paths. As shown, the column address register 20C has a binary '1' value that is propagated to energise all of the column paths in turn. The row address register (20R) has successive patterns (10, 100) for cyclically energising
80 each row address path once for each energisation of a corresponding column address path, i.e. will be clocked faster (twice or three times) than the column and address register.

Figure 9 shows selectably controlled input
85 circuitry for a logic gate site using reversible circuit elements 124. The gate 110 itself has two operative inputs 110A, 110B and one output 112. The operative inputs 110A, 110B can receive selectable direct connection paths
90 114A, 114B, 114C from neighbouring gate sites. Selectable connection path 114A can go to either or both of operative gate inputs 110A and 110B, by way of selectively conducting/non-conducting circuit elements 124X
95 and 124Y for signal pass purposes. Connection paths ·114B and 114C can be selectably connected only to 110A and 110B, respectively, through selectably conducting/non-conducting circuit elements 124B, 124C. In addi-
100 tion, selectably conducting/non-conducting circuit elements 124D and 124E are shown controlling access to 110A and 110B, respectively, from the connect bus row and column lines 152R and 152C. Figure 9 thus shows
105 one way for a two-input gate to receive signals from neighbouring gates (on 114A, B, C) and/or from direct connect bus lines (on branches 152R, C) it being understood that not more than one of the circuit elements 124X,
110 B, D and one of the circuit elements 124Y, C, D will be selected at any one time.

Provision for conduction/non-conduction selection, in the case of Figure 9, involves setting of the conduction state of active circuit
115 components (124) in the form of (MOS) field effect transistors as the selectable signal pass circuit elements 124. That is shown as relying, for site addressing, upon conjunction of row and column addressing signals on ad-
120 dress path branches 122R and 122C to transistor 160 whose gate is connected to the substrate (VSS). The transistor 160 is then operative to energise line 133 and thereby enable a set of floating gate transistors 132X,
125 Y, B-E for operation according to energisation states of branches 143X,Y,B-E from the program bus, respectively. Effectively, the floating gate transistors (132), when enabled over the line 133, can be selectively caused to store a
130 binary "0" or binary "1" according to applied

signal levels on the program bus producing
corresponding charge states. In turn, they de-
termine and maintain saturation (ON) and non-
saturation (OFF) of the selectable MOS transis-
5 tors 124. pull-up resistors 162 connected
from line 161 across the transistors 124
servo to maintain unselected ones of the tran-
sistors 124 in their non-saturated (OFF) state.
 Figure 9 does not show output branching on
10 a selectable basis back to the direct connect
bus lines, but that can readily be provided. As
for Figure 8, the gate sites of Figure 9 could
be reorganised with selection provisions for
local direct connection paths made in branches
15 from gate circuit outputs. The same is true
also for Figures 10, 11 and 18 to be de-
scribed. A further option would be to have a
selectable connection path between lines
152R and 152C before the transistors 124
20 and provision for selecting that connection,
i.e. a further combination of another signal-
pass transistor 124, a charge-trapping transis-
tor 132, and a program line 143.
 It is noteworthy that two-input gates are the
25 norm for present-day integrated circuit techno-
logy at least in relation to ULAs.
 Figure 10 shows a three-input NAND gate
210 of MOS type having operative inputs
210A, 210B, 210C, and output 212. Of those
30 inputs, 210B has a selectable connection for
path 214A, and 210A and 210C are shown
with alternative selectable connections to
paths 252R, 214B and 214C, 252C, respec-
tively, i.e. to direct connect bus and column-
35 adjacent gate inputs. In each case, that is
through selectably conducting/nonconducting
MOS transistors 224A-E. In like manner as for
Figure 9, the transistors 224A-E are shown
associated with floating gate transistors
40 232A-E, program branch lines 243A-E and ad-
dress line 233 from address transistor 260.
Additionally, however, Figure 10 shows fur-
ther selectable sigal-pass transistors 224G H
in branches from the gate output 212 to the
45 direct connect bus lines 252R, 252C, and cor-
responding floating gate transistors 232G.H
connected to the program bus branches
243G.H. Again, pull-up resistors 262 are
shown across the signal-pair transistors
50 224A-E, and will be similarly provided for
transistors 224G, H, see arrowed branches
from their control electrodes (gates).
 Gate sites of the Figure 9 type can be pro-
vided with selectable output branches in the
55 same way as for Figure 10.
 The circuits of Figures 9 and 10 provide for
selectably establishing conduction/non-conduc-
tion states of their signal-pass transistors
124, 224, and for charge-trapping transistors
60 132, 232 to serve as programmable/erasable
storage means that maintains desired conduc-
tion conditions for transistors 124, 224 on a
static basis.
 Further concerning Figures 9 (or 10), it will
65 be appreciated that the selectable connection

options could require current carrying capacity
of the transistor 180 (or 260) equivalent to
that of several of the transistors 132 (or 232).
typically up to four thereof. In terms of circuit
70 realisation on semiconductor material, usually
silicon at present, it may be advantageous, or
at least considered to be so, to avoid having
to form significantly different sizes of transis-
tor. A particularly compact implementation on
75 silicon is to have each of the transistors 132
(or 232) directly enabled in common from the
column select line 122C (or 222C) and each
associated with an individual transistor, which
latter transistors are further to be enabled in
80 common from the row select line 122R (or
222R).
 It is feasible to treat the program lines 143,
243 as a data bus and to treat switching tran-
sistors replacing the charge-trapping transis-
85 tors 132, 232 or even the selectable transis-
tors 124, 224 themselves (see later Figure
11). effectively as memory devices of dynamic
RAM type, i.e. requiring refreshment. Then,
the actual configuration of an overall circuit
90 using gate sites of the thus modified Figure
9/10 type could be stored in external mem-
ory, whether of permanent (ROM), semi-per-
manent or dynamic refreshed RAM, or reconfig-
urable EPROM type, or even of other type.
95 All that is required is a sequential addressing/-
gating facility to operate in cycles refreshing
each gate site hereof within its required re-
fresh time. Then, such chip circuitry, com-
pared with Figures 9 and 10, can actually be
100 simplified, not only by replacement of charge-
trapping transistors of floating gate or oxide
nitride sandwich types by normal MOS transis-
tors, but also by omission of the pull-up resis-
tors 162, 262. Such chips would, of course,
105 be reconfigurable at any time in the manner
discussed hereinbefore and, at least when
used in a computer system, it is feasible for
such chips to have alternative configurations
for the same function, and for a test pattern
110 or routine to be applied periodically to check
for any part of the chip going faulty, to iden-
tify same, and to go to an appropriate alterna-
tive configuration. A development of such a
chip is described for Figure 11.
115 Figure 11 shows a gate site circuit for
which the basic logic gate 110 is a two-input
NAND having inputs 110A and 110B as for
Figure 9. Subscripted references 160B, C, D,
E. F. X, Y are used for column address path
120 enabled transistors shown interposed in series
between the transistors 132' and 124' (oppo-
site channel type to Figure 9), with the pro-
gram branches 143 applied to the drains of
the former.
125 Further compared with Figure 9, Figure 11
shows an additional selectable input connec-
tion path 114F with associated connection
setting and selection transistors 124'F, 132'F
and 160F, which comes from the next but
130 one gate site output before it in its row, as

for further input 14F of Figure 2. Also, a further selectably conductive transistor 124'J is shown and, at 170, an associated connection of the logic gate input 110B to output of the transistor 124'J and to the gate output stage. Connection 170 serves for control purposes in stabilising the gate response to inputs 110A, 110B when only one of them has a signal, and thus obviates the need for the two pull-up resistors shown unreferenced in Figure 9. In addition, the path 170 and associated transistor 124'J permit a selected one of the paths 114A, 114B, 114F and 152R and a selected one of the paths 114A, 114C and 152C to be interconnected. That enables signals to be routed through such interconnection directly without traversing the logic gate. Also there are no pull-up resistors (162) for the selectable connection state setting transistors 124', which reflects operation of the Figure 11 circuitry in a dynamic mode rather than a static mode, i.e. on a refreshed basis, say from an associated ROM or RAM.

Reconfigurability of the Figure 11 embodiment is due to incorporating embodiments of the single signal-pass field effect transistor transmission gate of our above-mentioned separate patent application, one of which is to be seen within the dashed block labelled SPTT. There, the MOS transistor 124'C is the pass transistor in relation to line 114C and the switching transistors for refresh purposes are 160C and 132C. Operation is by reason of inherent gate capacitance to give state-storage and signal-pass in the same transistor, and it could be useful to enhance capacitance of the signal-pass transistor relative to other transistors, such as used (132,160) for switching purposes in selecting a signal-pass transistor for conduction. A p-channel transistor can be operated at +5 volts to −5 volts to avoid degradation at logic 'low' (0 volts) due to threshold effects (VT). Then, VDD1 and VDD2 would be at +5 volts and VSS would be at 0 volts for the logic gate but at −5 volts for the signal-pass transistors. For n-channel transistors, as shown, operation at acceptable speed results using voltage levels of +3 volts (effectively logic 'high' for the gate) and +5 volts at VDD1 and VDD2, respectively, and VSS at 0 volts.

The circuitry of Figure 11 can be represented, see Figure 12, by a two-input NAND gate 110 and two multiplexers 180A and 180B for inputs 114B, 114F, 152R and 114A, 114C, 152C, respectively. Input 114A is shown, as in Figure 9 and 11, to be available also to the multiplexer 180A. Also, and in connection with the fourth gate site interconnection 114F from the next but one preceding gate site, it may be found to be advantageous (in avoiding unecessary cross-overs) for the inputs 114A and 114F to be alternately interchanged along each row of gate sites, see Figure 13 and Figure 2. Figure 12

also indicates at 170 the capability for inputs to go from one multiplexer to the other without traversing the logic gate 110. For convenience, only one set of inputs are shown going to the multiplexers 180A, 180B for selection purposes. As indicated in Figure 13 by blocks 200 (GMUX is short for multiplexed gate) each gate site can be considered as including the logic gate proper (110) and the multiplexer parts (180A, 180B).

The Figure 13 diagram is at a corner of a configurable gate array and is further useful in relation to the following description concerning input/output provisions.

Turning to input/output provisions, Figure 14 shows a central rectangular area occupied by reconfigurable logic gate array 300, and peripheral cells 310A, B, C, D outside that area, actually at each edge. Logic circuit sites of the gate array may be as for Figure 11, and corners of the array as for Figure 13. Outside the peripheral cells 310, are conduction buses 320A, B, C, D going about corners of the chip and branched from conduction paths going between edge input/output pins or pads 326A-D and the peripheral cells 310A-D. The peripheral cells 310 A-D serve in communication between those pads 326 and array input and output lines at each edge, though it will be noted that buses 320A-D do allow flexibility in permitting pads 326A-D at any one side of the chip to be inputs/outputs alternatively for the peripheral cell at the next adjacent side of the chip.

There are more logic array input/output lines than there are pads 326, typically a ratio of more than ten to one. One envisaged chip of 50 × 40 logic gates has 520 array lines and 40 pads. The aim, however, is simply to suitably relate necessary array lines with a convenient, preferably conventional, number of pads (or pins) for integrated circuits. patterns of connections of the pads to groups, respectively, of the array lines are preferably formed at edges of the array 300.

In Figure 14, peripheral cell 310A services row inputs/outputs from one side of the gate array 300 (left as shown) and peripheral cell 310D services column inputs/outputs from another side of the gate array 300 (bottom as shown). Peripheral cells 310C and 310B similarly service the other array sides, respectively. Regarding the pads 326, the peripheral cell 310A services all of those at the adjacent chip side directly, and half of those at each adjacent chip/array side are directly serviced by other peripheral cells 310D and 310B. The other peripheral cells are similarly organised.

In Figure 13 it will be noted that alternate ones (odd-numbered) of the column array lines (D) each serve only inputs to gates of the edgemost row of the array 300 (Figure 14), and that other ones (even-numbered) serve outputs of the same gates but can further serve inputs of the next row of the array. For

row array lines (L), the pattern reflects the
fact that the gates of adjacent rows alternate
in direction. Every third row (L1, L4) array line
serves only an input of the end gate of alter-
5 nate rows, the next lines (L2, L5) serve only
an input of the second to end gate of the
same rows, and the next lines (L3) can serve
both output from the end gate of the other
rows and alternative input to the end gates of
10 flanking rows. The capability to get directly to
both edge-most gates of the array and those
gates next to them is advantageous. However,
it will be appreciated that there is much.
deeper possible access, whether by the afore-
15 mentioned direct connect bus system or by
going into and out of multiplexer parts of gate
sites or by traverse of gates thereof.
    A diagrammatic representation of a periph-
eral cell 310 is shown in Figure 15. see array
20 lines DA, QA representing inputs/outputs of
logic gates and pad lines PA. Each peripheral
cell is a set of subcells one for each pad PA,
each subcell being as shown (330) in Figure
16 from which the purpose of other lines of
25 Figure 15 will be appreciated.
    In Figure 16, subcell 330 actually provides
for its pad line (PA) to serve as either input or
output in a particularly efficient and advan-
tageous way. The subcell 330 has a tristate
30 inverter 332 and two inverting transistors
(334,336). 332 and 334 are connected to
gate lines QA, DA of the logic gate array 300
for input and output purposes relative thereto
and to the corresponding pad PA. 336 deter-
35 mines the input/output service status of the
subcell, being connected between circuitry
338 and control for the inverter 332. The cir-
cuitry 338 has two series connected MOS
transistors (unreferenced) having their gates
40 connected for coincident signal enablement
(address lines R4, C5) and their substrates
connected to logic voltage high, so as to pass
a bit signal for determining the service state
of the subcell (shown from line DBO of inpu-
45 t/output configuring data bus or the aforesaid
program bus). The subcell service state (input
or output) is set and maintained on a dynamic
basis relying on input capacitance of the inver-
ter 332 in much the same way as self-capaci-
50 tance is used in the single-pass transistors
124 of Figure 11.
    In operation, the subcell 330 has its tristate
inverter 332 controlling transmission from the
chip through the pad PA (output) or for block-
55 ing such transmission when the inverter 332
"floats" and there is transmission into the
chip from the pad via the inverter 334 (input).
Additionally, and most advantageously, there
is the capability of transmission between the
60 array lines (DA, QA) which can be used by
the logic gate array if required.
    It is possible to replace the inverter 332 by
a NAND gate so as at least to be able to get
control or data signals from the logic array for
65 outputting via the pad (PA), say to an external

computer or other system on a tristate basis
where array configuration conditions can de-
termine input or output or neither,
    It is, of course, possible to control the inpu-
70 t/output status of any subcell of each periph-
eral cell by program and/or from ROM, which
is particularly advantageous in conjunction with
reconfiguration potential of chips hereof, i.e.
any pad can be input or output and has a
75 considerable choice of immediately accessible
logic array gates, though obviously not limited
thereto.
    It will have been noted that there is direct
correlation of one pair of array input and out-
80 put lines (DA, QA) to one pad (PA), ignoring
pad interconnections 320 of Figure 14.
Another feature hereof is thus that the array
lines (QA, DA) are not actual array lines (L, D)
but represent output connections (DA) to sets
85 thereof selected on a basis intended to max-
imise efficiency in view of some inevitable
loss of choice, though all inputs (QA) will go
to all available inputs of the edge of the ar-
rays. That, connection scheme is, of course, a
90 matter for judgement by chip designers but
should, we believe, take into account that less
input/output flexibility is required near corners
of a gate array then medially thereof. In fact,
some lines it serves will have no connections
95 to the peripheral cell, perhaps (for columns,
but not necessarily rows) on a basis missing
alternate ones closest to the corner, but only
every fourth otherwise, and grouping interven-
ing three actual array lines appropriately to
100 speed access in an alternative way relative to
the two halves of side pads PA and then their
interconnections 320.
    Figures 9 to 11 hereof have all been con-
ceived for field effect chips, specifically
105 CMOS. Figure 18 shows gate site circuitry for
a bipolar chip.
    In Figure 18, a bipolar NAND gate com-
prises a transistor 410 in combination with
transistors 424 also serving as selectable in-
110 puts thereto. Gate output 412 is shown
buffered (413) in generally conventional man-
ner. Control of the conduction states of the
transistors 424 is shown at 420 by way of
equivalents to SCR-type devices in turn con-
115 trolled by respective transistors 422. Similar
circuitry, shown with primed references, is
used for branches from the output 412 of the
gate but relative to individual transistors 430
to give required separate outputs to the direct
120 connect bus (452).
    Complementary transistors 420A, 420B are
shown each having its base connected to the
collector of the other, so as to be triggerable
(under suitable applied voltage conditions) by
125 a pulse signal at one of its base-collector con-
nections and go to a prescribed voltage level.
That level will then persist after triggering until
applied voltage conditions are changed.
    The transistor 422 serves to apply such
130 triggering on an addressed basis, in this case

by being made momentarily conducting by sig-
nals from a unique pair of one of row follow-
ing lines X1-X3 and one of column following
lines Y1-Y3 of coded address buses of the
5 logic gate array, i.e. in the manner envisaged
with reference to Figure 17B.

It is noted that the transistors 422 and trig-
gerable arrangements 420 operate without re-
quiring separate address (enabling) signals and
10 configuring signals. Moreover, whilst the tran-
sistors 424 clearly operate on a selectable
signal-pass basis, they actually form parts of
the NAND gate itself.

It is also noteworthy that the NAND gate of
15 Figure 18 will operate as a true six-input gate
for all of the direct connect inputs 414A, B,
C, F and the direct bus connections 452R,
452C. (That possibility was implicitly envi-
saged for the Figure 8 embodiment, though
20 the use of field effect transistors for selecting
conduction purposes may make the Figure 9
or 11 arrangements more practical in relation
to two-input gates).

Futhermore, the output branch transistors
25 430 give an inverted output (relative to gate
output 412), and are of open-collector confi-
guration enabling what is in effect a wired-OR
type output capable of multiple line driving.

Before considering system aspects arising in
30 utilisation of reconfigurable logic circuit chips
hereof, it is deemed useful to point to several
features generally characteristic of presently
envisaged embodiments of this invention.
From what has been described relative to the
35 drawings, it will be apparent that selectability
may be achieved by providing a fusible link or
diode or similar element in each selectable
connection which, by the application of an ap-
propriate signal, can be disabled thus causing
40 a single irreversible change from a conducting
to a non-conducting state. In other cases, the
selectability may be achieved by incorporating
an active circuit component such as a transis-
tor in the connection path in such a manner
45 that its conducting or non-conducting state
determines the state of the connection path
on a reversable basis, selection signals being
applied to the active circuit component to
control its state as required. Control of the
50 transistor or similar element may be on a sta-
tic bais such that changes of state require a
special operation, or on a dynamic basis
where desired states require to be refreshed
during normal system operation but can like-
55 wise be changed, or on a static basis for
which changes can also be made as part of
normal system operation.

Also, even if less sophisticated input/output
arrangements are employed on a chip, and
60 even if much more complex logic circuits are
implemented, it is not expected that any logic
circuit will be directly connected (14) to more
than 5% of the total number of logic circuits
present, generally less than 1%, even lower
65 than 0.01% for simple logic gate circuits. Typ-

ically, the number of connected logic gates
will be ten or less often five or less. Also, it
is expected that chips hereof will contain at
least 500 logic circuit sites, advantageously
70 more than 1000, and that each logic circuit
site will occupy less than 0.2% of the area
devoted to such sites. Our preference is for
less than 25% of each logic circuit site to be
occupied by its actual logic circuit, which is
75 demonstrated in Figures 8, 9, 10, 11 and 18
by relative numbers of transistors in actual
gate circuits and in associated connection path
selection circuitry.

Figure 19 shows a typical possible overall
80 chip layout, effectively adding to Figure 14 the
row and column addressing shift registers
520R and 520C, a data latch 530, clock 540,
an address register 550, and timing control
560.
85 The address register 550 and the data latch
530 are shown with associated buses 552
and 532, respectively, to edges of the chip
where there will be pins or pads separate
from the input/output pins or pads 326. They
90 are used for dynamic chips in effecting re-
freshing, when the address register will be a
counter cycling through part of a ROM or
RAM storing the configuration of the chip, and
the data latch successively stores binary
95 words from the ROM or RAM that succes-
sively define which selectable corrections are
required at addressed logic circuit sites. Tim-
ing signal lines are shown going to the coun-
ter 550, the latch 530, and the row and col-
100 umn select registers 520R,C. These provisions
are also used in loading configurations under
control of the configurable chip itself. There
may be two control signals to the address
counter 550, one for counting at chip-con-
105 trolled loading or refreshing, and the other for
read/write control to allow the address coun-
ter also to be loaded through the bus 552.

We have previously referred to electronic
system aspects of this invention arising from
110 use of configurable chips, particularly chips
that are reconfigurable at or near normal logic
signal levels and speeds.

Figure 20 shows association of a reconfigu-
rable chip 600 with a RAM 602 communicat-
115 ing with the chip 600 by an address bus 604
and by a two-way data bus 606. Selection
means is indicated at 608 for causing the
RAM 602 to be loaded or reloaded with confi-
guration data for the chip 600. Utilisation
120 means is shown at 620 and will usually sup-
ply input signals for processing by the chip
600 as well as take signals representing re-
sults of such processing. Such signals will be
on bus 622 connecting to input/output pins
125 (326) of the chip.
Reconfiguration may be to different pur-
poses or to the same purpose, and refreshing
may be required. Reconfiguration for different
purposes can be controlled by a sequencer as
130 part of the selection means 608. That can be

in relation to several configurations resident in
the RAM 602, or in relation to configurations
that require sequential loading into the RAM
602. The selection means is shown as part of
5 host or associated apparatus 610 that will
normally further include at least configuration
data (610B) and addressing (610A) facilities
for the RAM 602 over extensions 606A and
604A of the buses 604. It is the case, of
10 course, that the chip 600 will usually include
provision itself for addressing the RAM 602
over the bus 604.
   Similar considerations apply to reconfigura-
tion to the same purpose, when it is most
15 likely that the RAM 602 will contain at least
some alternative, or back-up, configurations.
Test patterns can also be stored in the RAM
602 or supplied from the apparatus 610.
   Figure 21 shows a generally similar arrange-
20 ment of reconfigurable chip 600 and RAM
602 connected by address and data buses
604, 606. However, multiplexers are shown at
612, 614 to control whether the chip 600 has
access to the RAM 602 over buses 604, 606
25 or whether configuration buses 616, 618 have
access to the RAM 602. That can permit
rewriting of the RAM 602 without interrupting
operation of the chip 600.
   Also, specific provision is shown for the
30 chip 600 to address different parts of the
RAM 602 (corresponding to different configu-
rations for the chip) over further address lines
630 indicated as coming from part of configu-
rable input/output provisions of the chip 600.
35 That further results effective control of confi-
guration selection by means connected to the
input/output system 622, as well as in accor-
dance with a condition otherwise arising in the
chip 600. It should further be appreciated that
40 the address bus 604 could have its most sig-
nificant lines serving the purpose of lines 630,
say coming from a suitable latch section of
the address register (550 in Figure 19) that
does not respond to counting cycles required
45 for any refreshing of a currently resident chip
configuration.
   Further, Figure 21 shows provision for oper-
ation as one of a plurality of chips making up
an electronic system. An identification decoder
50 is shown at 640 connected to receive se-
lected (usually most significant) lines 642 of
the configuring bus 616. If the decoder 640
recognises that its associated chip/RAM com-
bination 600/602 is concerned, it will appro-
55 priately enable its output lines 644 and 646
to cause the multiplexers 612, 614 to switch
the RAM 602 from buses 604, 606 to confi-
guring buses 616, 618. Also, decoder output
line 648 will put the RAM into write mode.
60 Decoder output 650 may disable the chip 600
if there could be a clash with refreshing a
dynamic chip 600 or other call from chip 600
for a new configuration. Such clashes should,
however, be avoidable by suitable system tim-
65 ing, when the current configuration could be

rewritten to the first configuration section of
the RAM 602 and the line 650 used to reset
the lines 630 or writable address register
latch.
70 A plural chip system is indicated in Figure
22 in which each of blocks 800 will comprise
a reconfigurable chip, each usually also with
an associated RAM. The chips are intercon-
nected at 805 via their above-mentioned inpu-
75 t/output provisions, and provision is made for
input data from source 820 over bus 825 and
for output data to utilisation means 810 over
bus 815. Such a chip system is clearly
capable of serial processing where the chips
80 are differently configured and of parallel pro-
cessing where the chips are similarly confi-
gured, and of desired combinations of serial
and parallel processing. One or more of the
chips may be devoted wholly or partly to con-
85 trol purposes, though some host apparatus or
system will usually be provided and itself may
include the separately indicated signal supply
means 820 and utilisation means 810.
   It is believed to be advantageous for plural
90 chip systems to be provided on as few
printed circuit boards as possible, hence
showing dashed outline 830 in Figure 22.
Such boards may contain more, advantage-
ously very many more, reconfigurable chips
95 than are shown in Figure 22, and may further
contain other chips constituting the host sys-
tem or a part or parts thereof.
   Figure 23 shows a preferred printed circuit
board 930, which is generally similar to that
100 of Figure 22 for connections 905 between in-
put/output provisions of its configurable chips,
some of which may be used at least partly
simply for passing signals between input/out-
put provisions thereof. In addition, however,
105 Figure 23 shows a configuring address (914)
and data (918) bus system for loading RAMs
associated with each configurable chip in the
manner of Figure 21. i.e. each block 900 cor-
responds to Figure 21. Then, the configuring
110 bus system 914, 918 can identify any block
900 (via a decoder as shown at 640 in Figure
21) and reload its RAM, if required without
any other block 900 to branch chip needing
to be disabled. It is even possible to reload
115 RAM of a block 900 without stopping its own
chip so long as timing assures no clash with
that chip's access requirement to its associ-
ated RAM and/or the currently used configura-
tion is either not overwritten or is prewritten
120 to the RAM with accompanying rewriting of
the address register of the chip or at least the
supply to the lines 630 of Figure 21.
   The configuring bus system 914, 918 is
shown coming from an off-board facility 960
125 constituting a source or library of chip confi-
gurations and normally comprising at least a
desk-top computer with disc store. That facil-
ity 960 may be separate from the source 920
of data (over input bus 925) for processing by
130 the chips of logic blocks 900 and/or from the

utilisation means 910 receiving processing re-
sults over bus 915, or may be part of an
overall computer system including either or
both of 910,920. Typical source means 920
5 will include a disc store with output RAM,
and/or a data circuit terminal, and/or a com-
puter system, etc. Similarly, a typical utilisa-
tion means 910 will include a disc store an-
d/or a printer and/or a visual display unit, etc.
10 It will be recalled from Figure 14 that one
configurable chip hereof affords ten input/out-
put pads or pins at each side. Using such
chips in the logic blocks 900 of Figure 23, a
conventional 8-bit wide data flow can readily
15 be provided at 905 between logic blocks 900.
Other lines could also be so interconnected
for inter-block control purposes and/or at
least some of them collected into a bus tra-
versing all of the logic blocks 900 for global
20 control and/or logic block addressing pur-
poses, see 870 in Figure 23.
      It will be appreciated that Figure 23 is not
intended to indicate any particular size of
board 930 and associated population of logic
25 blocks 900, there being several break lines in
Figure 23. Also, the snaking paths of the con-
figuring bus 914, 918 and global bus 970
could be of other layout, and the configuring
address (914) and data (918) buses could be
30 separate rather than superposed. Boards of
Figure 23 could, of course, be connected to-
gether into an even larger system, say using a
mother-daughter board arrangement.
      As data processing apparatus, a system
35 (such as shown in Figure 23) utilising a plural-
ity of configurable chips has great potential,
whether the chips are as in Figures 9-19
hereof or otherwise.
      The data processing power of the system is
40 demonstrable relative to conventional pro-
grammed computer systems. Inherently, every
programmed computer deals with program in-
structions in an essentially sequential manner.
That is, of course, why computer simulations
45 of purpose-built electronic apparatus tend to
be very slow compared with the actual appa-
ratus simulated. Both of electronic computers
and other purpose-built electronic apparatus
utilise electronic logic chips, and the compari-
50 son in terms of speed is between the speed
at which such chips can operate and transfer
electric signals between themselves, and the
number of cycle times of a computer required
to execute the number of program instructions
55 that need to be processed for the simulation.
One way to increase data processing capabil-
ity, in certain suitable circumstances, is to op-
erate component computer subsystems over-
lapped or in parallel. However each of such
60 subsystems has the same characteristics as
any programmed computer, i.e. it operates se-
quentially on program instructions. Using con-
figurable chips, however, the desired functions
can each be set up by configuring the chips
65 whose individual and collective configuration

then constitute a special-purpose logic system,
which will operate at electronic switching/-
transmission speeds rather than at speeds re-
lated to computer cycle times. However much
70 execution of program instructions can be ef-
fectively overlapped and cycle times reduced
(as is done for powerful computer systems
performing millions of instructions per sec-
ond), there is still sequentiality, i.e. all pro-
75 gram instructions can never be executed si-
multaneously. In effect, of course, simulta-
neous performance is what applies for confi-
gured chips in a system hereof.
      A single reconfigurable chip of the Figure 11
80 type using 3-micron CMOS fabrication can
have at least 2,000 logic gates, and it should
be possible to increase to over 8,000 gates
using 1 micron CMOS fabrication. We can
achieve utilisation of over 60% of gates on
85 such chips in particular useful configurations. It
is possible to calculate a number (N), based
on the actual number of executed program in-
structions required to execute a computer pro-
gram simulating the chip configuration con-
90 cerned, and correlated with the cycle times of
the computer concerned and the configured
chip (say at 5MHz—15MHz operation for the
latter), so as to express execution time of a
simulation program for any particular computer
95 in terms of a multiple of the time taken for a
configured chip (i.e. actual logic) to operate.
      It is possible to calculate numbers (N1, N2
etc.) for all of the configurable chips of a plu-
ral chip system, say of the Figure 23 type.
100 For M configurable chips operating wholly seri-
ally in processing input data according to their
individual and collective actual configurations,
a programmed computer would take N1 + N2
+.....+ NM times as long as to perform the
105 same function. Moreover, the Figure 23 sys-
tem can produce output at every cycle after
the Mth. For M chips operating in parallel only
one cycle of a Figure 23 system is required
(at least ignoring any requirement to avoid
110 "clashes" between chip outputs, which could
be rare in investigation of different parts of a
spectrum of data for particular features). Then,
the "improvement factor" would approach
M(N1 + N2 +.....+ NM), and could not re-
115 duce by more than M even if there were con-
tinuous "clashes" of chip outputs requiring se-
parate cycles to go to utilisation means.
      Importantly, reconfiguration from RAMs as-
sociated one with each configurable chip takes
120 only a RAM read time (equivalent to a load or
refresh cycle time). Even for reloading RAMs,
only a RAM write followed by a RAM read is
required, and that can be managed efficiently
by rewriting RAMs without interruption of cur-
125 rent chip operation as each RAM could con-
tain many configurations (each requiring one
binary word per gate of the chip).
      It will be apparent that the number N can be
converted, for any particular computer com-
130 parison, into equivalents to the rate at which

instructions are performed by the computer concerned. Systems must as in Figure 23 can thus represent inexpensive equivalence to very powerful and expensive computers. Effectively,
5   a Figure 23 system is actual electronic logic for every overall configuration and can be reconfigured by the equivalent of programming.

CLAIMS
10   1. A configurable semiconductor integrated circuit which, as-made, comprises an area thereof formed both with a plurality of logic circuits at discrete sites, respectively, and with a restricted signal translation system between
15   inputs and outputs of the logic circuits affording direct connection paths each selectable as to its conduction state, those paths extending, for each of said logic circuits, from its output to inputs of a first set of others of said logic
20   circuits and to its inputs from outputs of a second set of others of said logic circuits, all of the sets (for all of the logic circuits) each being unique.
      2. An integrated circuit according to claim
25   1, wherein the discrete sites are distributed over said area and interspersed with the direct connection paths which traverse said area between the sites.
      3. An integrated circuit according to claim
30   1, wherein the discrete sites are distributed over said area in a pattern representing a substantially uniform density of sites within the area and the direct connection paths traverse between the sites.
35   4. An integrated circuit according to any preceding claim, wherein, for each said logic circuit, the first and second sets include at least one said logic circuit in common.
      5. An integrated circuit according to any
40   preceding claim, wherein, for each said logic circuit, at least one of the first and second sets includes a said logic circuit not in common.
      6. An integrated circuit according to any
45   preceding claim, wherein some of the inputs and outputs of some of the logic circuits have selectable connection paths extending to input/output means for servicing the plurality of logic circuits, and wherein each of the sets for
50   at least the remainder of the said logic cicuits comprises at least three others of said logic circuits.
      7. An integrated cicuit according to claim 6, wherein each of the sets includes less than
55   5% of the total number of said plurality of logic circuits.
      8. An integrated circuit according to claim 6 or claim 7, wherein, at least for each said remaining logic circuit, the first and second
60   sets include two said logic circuits in common.
      9. An integrated circuit according to claim 6, 7 or 8, wherein, at least for some said remaining logic circuit each of the first and
65   second sets includes two gates not in com-

mon with the other.
      10. An integrated circuit according to claim 5 or claim 9, wherein considering said logic circuits as arranged in rows and columns,
70   each said logic circuit not in common is in the same row as the logic circuit concerned, each of the logic circuits next adajacent to it in the same row being in different ones of the first and second sets.
75   11. An integrated circuit according to claim 10, wherein others of said logic circuits not in common comprise next-but-one said logic circuits in the same row.
      12. An integrated circuit according to claim
80   4, wherein, considering said logic circuits as arranged in rows and columns, each said logic circuit in common is next to and in the same column as the logic circuit concerned.
      13. An integrated circuit according to claim
85   12, wherein at least some of said logic circuits that are next adjacent in columns are oppositely formed at their said sites in the sense of access to their outputs.
      14. An integrated circuit according to claim
90   13, wherein the oppositely formed logic cicuits alternate in each column but are all similarly formed in each row.
      15. An integrated circuit according to any preceding claim, wherein further input connec-
95   tion paths to the logic circuits are each selectable in a manner similar to said direct connection paths.
      16. An integrated circuit according to any preceding claim, wherein further output con-
100 nection paths of the logic circuits are each selectable in a manner similar to said direct connection paths.
      17. An integrated circuit according to claim 16, wherein said further ouput connection
105 paths are branched from the first-mentioned outputs of logic circuits.
      18. An integrated circuit according to claim 15, 16, or 17, further comprising another signal translation system having at least one
110 other direct connection path of an extent traversing more of said sites than can be reached through any one said set of direct connection paths, and wherein said further input connection paths, and further output con-
115 nection paths where present, constitute branches from said other direct connection path.
      19. An integrated circuit according to claim 18, wherein said further input connection paths, and further output connection paths
120 where present, constituting said branches are two per logic circuit, and said other signal translation system has plural said other direct connection paths some extending between rows of a matrix array of said sites and oth-
125 ers extending between columns of said sites, said further input connection paths at each said site, and further output connection paths where present, being branched to a unique corresponding combination of one each of the
130 row-following and column-following ones of

said other direct connection paths.

20. An integrated circuit according to claim 18 or 19, wherein at least some of said other direct connection paths comprise discrete segments.

21. An integrated circuit according to claim 20, wherein the discrete segments are interconnectable only via the logic circuits.

22. An integrated circuit according to claims 19, 20 or 21, wherein row-following and column following ones of said other direct connection paths are connectable to each other via a said logic circuit for which said unique combination applies.

23. An integrated circuit according to any one of claims 18 to 22, wherein row-following and columnfollowing said other direct connection paths are selectably connectable together without traversing any said logic circuit.

24. An integrated circuit according to any preceding claim, wherein all selectable connection paths each include a circuit element dedicated thereto and whose as-made conduction state can be changed by application of configuring electrical signals or signal conditions.

25. An integrated circuit according to claim 24, wherein each said circuit element has associated further circuitry by which it is conditioned for configuration, and wherein conducting address paths traverse said area for energisation in conditioning the further circuitry of circuit elements to be configured.

26. An integrated circuit according to claim 25, wherein said circuit elements and associated further circuitry for all inputs of each logic circuit, and outputs where selectable, are disposed adjacent to the corresponding gate circuit and included within the corresponding said site.

27. An integrated circuit according to claim 26, wherein more of each said site is devoted to formations of its said circuit elements and associated other circuitry than to formation of its logic circuit.

28. An integrated circuit according to claim 27, wherein less than 25% of each said site is devoted to formation of its logic circuit.

29. An integrated circuit according to claim 26, 27 or 28, further comprising logic circuit site addressing means having said address paths operating on a coincident basis to identify each said site and, when jointly energised, establish conditions for each said further circuitry thereat whereby each selectable connection path will be responsive to said configuring electrical signals or signal conditions.

30. An integrated circuit according to claim 29, further comprising program conducting paths corresponding in number to the number of selectable connection paths at a said site and serving to cause application of said configuring electrical signals in respect of selected said connection paths.

31. An integrated circuit according to claim 30, wherein said program conducting paths

traverse throughout the logic circuits and are branched to each said site.

32. An integrated circuit according to claim 29, wherein said coincident current address paths are in plural groups and each selectable connection path at each site has coded connection thereto for generating configuring signal conditions.

33. An integrated circuit according to any one of claims 29 to 32, further comprising sequential energising means for said addressing means.

34. An integrated circuit according to any preceding claim, wherein said sites each occupy less than 0.2% of said area.

35. An integrated circuit according to any preceding claim, wherein said area comprises at least 500 said sites.

36. An integrated circuit according to any one of claims 25 to 33, wherein a said circuit element comprises a conducting link that will be rendered irreversibly non-conducting by a said configuring electrical signal applied thereto.

37. An integrated circuit according to claim 36, wherein each said further circuitry includes an active circuit device connected in series with its associated said conducting link, said active circuit device being rendered conducting by signals from said address paths in order to pass a said configuring electrical signal if applied.

38. An integrated circuit according to claim 37, wherein each said further circuitry also includes another connection in series with the conducting link that determines actual conduction of said energising electrical signal when set to a particular voltage level by an appropriate further signal.

39. An integrated circuit according to any one of claims 25 to 33, wherein a said circuit element comprises an active circuit component having a conduction control connection and that remains reversible as to its conduction state after application of a said configuring electrical signal.

40. An integrated circuit according to claim 39, wherein the active circuit component comprises a transistor.

41. An integrated circuit according to claim 39 or claim 40, wherein each said further circuitry includes an active circuit device connected to the conduction control connection of its associated said active circuit component, said active circuit device being rendered capable of conduction using signals from said address paths so as to provide a said configuring electrical signal condition when the active circuit device is actually rendered conductive.

42. An integrated circuit according to claim 41, wherein the active circuit device will remain conducting after being rendered conductive by a pulse signal.

43. An integrated circuit according to claim

37, 38, 41 or 42, wherein the active circuit
device comprises a transistor.
    44. An integrated circuit according to claim
43, wherein the transistor is of field effect
5 type.
    45. An integrated circuit according to claim
44 with claim 43, wherein the transistor is of
charge trapping type.
    46. An integrated cicuit according to claim
10 45, wherein active circuit components have
voltage control resistors connected to hold
them non-conducting if not selected for con-
duction.
    47. An integrated circuit according to claim
15 42 or claim 43, wherein said circuit element
requires repeated application of said configur-
ing electrical signal in order to maintain its
configured conduction state.
    48. An integrated circuit according to claim
20 47, wherein the active circuit component is a
field effect transistor relying on its own capa-
citance to remain adequately conducting be-
tween periodic applications of said configuring
electrical signal.
25   49. An integrated circuit according to claim
48, wherein the field effect transistor is n-
channel and operating voltages are at and be-
low normal logic "high" voltage.
    50. An integrated circuit according to claim
30 42, wherein the active circuit component is a
bipolar transistor and its said further circuitry
is of triggerable conduction state setting type.
    51. An integrated circuit according to claim
50, wherein said further circuitry comprises
35 the bipolar circuit equivalent of two comple-
mentary transistors interconnected base-to-col-
lector.
    52. An integrated circuit according to claim
51, wherein said further circuitry further com-
40 prises a bipolar transistor controlling a voltage
to a path to a said base-to-collector connec-
tion and serving for setting a voltage condition
required for switching of the further circuitry
then setting the active circuit component to
45 conduction.
    53. An integrated circuit according to any
preceding claim, wherein each logic circuit is a
single-output logic gate for performing a single
inverting logic function.
50   54. An integrated circuit according to claim
53, wherein the logic circuits each have a les-
ser number of operative inputs than there are
selectable said connecting paths for input pur-
poses, and those selectable connecting paths
55 are in groups each connected to a different
operative input for selection of one said path
of any group relative to the corresponding op-
erative input.
    55. An integrated circuit according to claim
60 54, wherein at least one of the selectable
connecting paths for input purposes is in more
than one said group.
    56. An integrated circuit according to claim
53, 54 or 55, wherein all of the logic circuits
65 comprise similar logic gates.

    57. An integrated circuit according to any
one of claims 53 to 56 comprising NAND
logic gates.
    58. An integrated circuit according to claim
70 57 with claim 50, wherein the bipolar transis-
tor constituting the active circuit component
has its control electrode connected in the
emitter-collector circuit of an output transistor
of the logic gate.
75   59. An integrated circuit according to any
preceding claim, further comprising input-out-
put circuitry formed with communication to
logic circuit inputs and outputs extending from
said area.
80   60. An integrated circuit according to claim
59, wherein said input-output circuitry com-
prises cells each servicing a different side of a
matrix array of said logic gates.
    61. An integrated circuit according to claim
85 60, wherein each cell comprises subcells con-
figurable between first and second states in
which signals can go to logic circuit inputs or
come from logic circuit outputs, respectively.
    62. An integrated circuit according to claim
90 61, wherein subcells connected to outputs of
edge-most ones of the logic cells are further
connected to inputs of the next ones of the
logic circuits.
    63. An integrated circuit according to claim
95 61 or claim 62, wherein each said subcell is
connected to a unique group of logic circuit
inputs and outputs and there are fewer sub-
cells than serviced logic circuit inputs and out-
puts.
100   64. An integrated circuit according to claim
61, 62 or 63, wherein inputs and outputs of
logic circuits closest to corners of said array
are connected into fewer said groups.
    65. An integrated circuit according to any
105 one of claims 60 to 64, further comprising
conducting paths interconnecting chip connec-
tions of selected subcells on two adjacent
sides of the array.
    66. A configurable semiconductor integrated
110 circuit in the various embodiments substan-
tially as herein described with reference to and
as shown in Figures 1 to 19 of the accom-
pany drawings.
    67. An electronic system comprising a re-
115 configurable semiconductor integrated circuit
having a plurality of logic circuits for which
alternative configurations involving different in-
terconnections of inputs and outputs of the
logic circuits enable different performance of
120 some overall system function, and means for
presenting to the reconfigurable integrated cir-
cuit configuration—defining signals to which
the reconfigurable integrated circuit is respon-
sive to adopt a desired configuration.
125   68. A system according to claim 67, further
comprising means for utilising signals from the
reconfigurable integrated circuit.
    69. A system according to claim 67 or
claim 68, wherein the means for presenting
130 includes a store system readable to provide

said configuration representative signals on an
alternative basis for each of different configu-
rations, and further comprising means for ad-
dressing the store system according to which
5 configuration is required.

70. A system according to any one of
claims 67 to 69, wherein alternative configura-
tions are for the same overall system function
performed in different ways.
10   71. A system according to any one of
claims 67 to 70, wherein alternative configura-
tions are for different overall system functions,
respectively.

72. A system according to any one of
15 claims 67 to 71, comprising a plurality of said
reconfigurable integrated circuits with bus sig-
nal translation provision between them for se-
rial/parallel processing in relation to overall
system function.
20   73. A system according to claim 72 with
claim 69, wherein each reconfigurable inte-
grated circuit has its own store.

74. A system according to claim 73, com-
prising further bus signal translation provision
25 for addressing and writing configuration data
to each store.

75. A system according to any one of
claims 67 to 76, wherein each reconfigurable
chip is as claimed in any one of claims 47 to
30 66.

76. An electronic system substantially as
herein described with reference to and as
shown in Figures 20 to 23 of the accompany-
ing drawings.